

LCFC Confidential

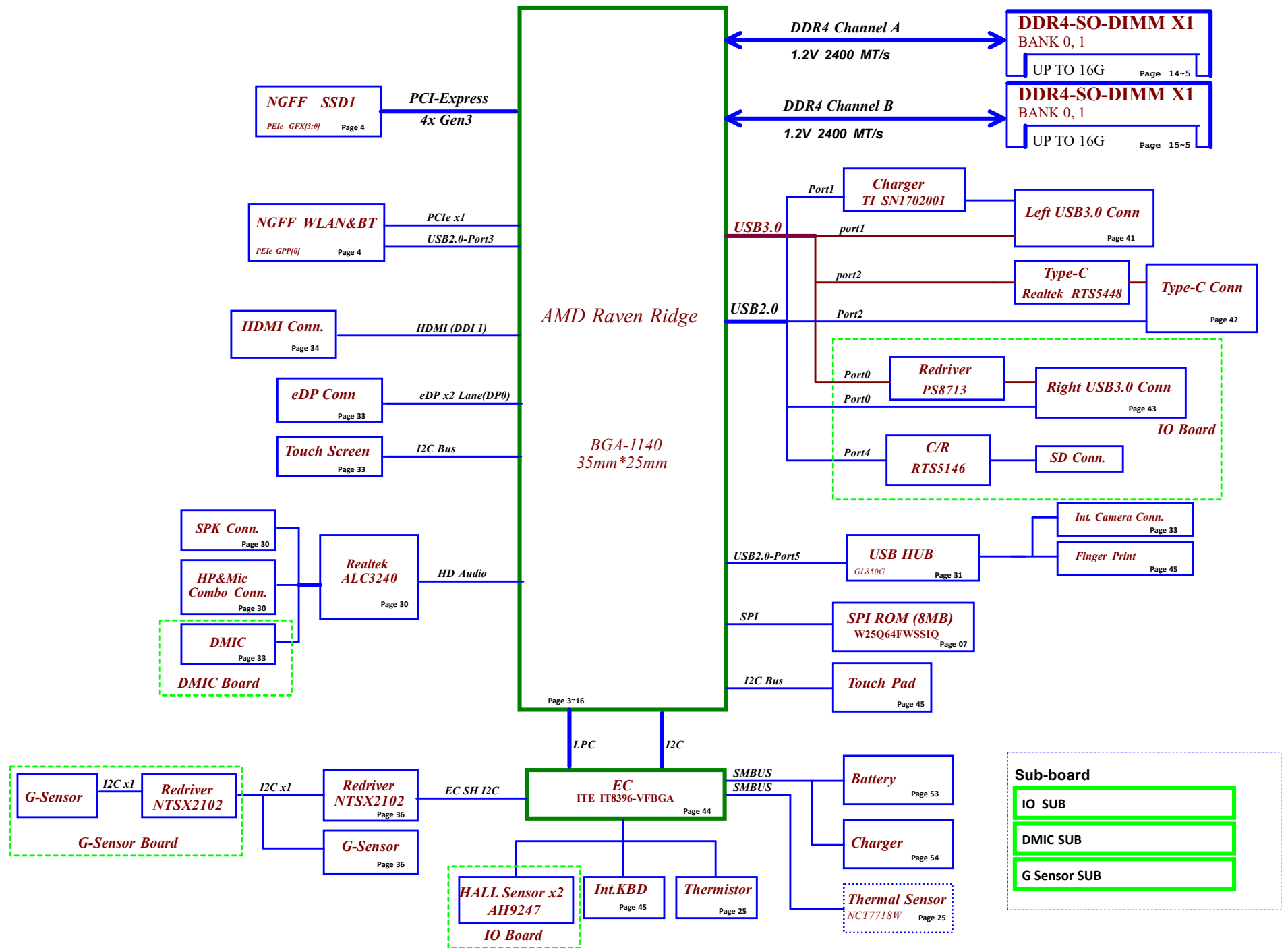
NM_B781 MB Schematics Document

AMD Raven Ridge with DDR4

2017-11

REV:1.0

Security Classification	LC Future Center Secret Data		Title			
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page		
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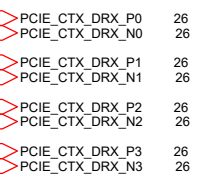
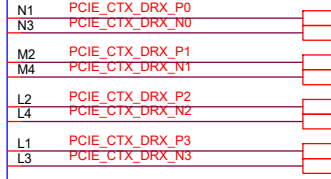
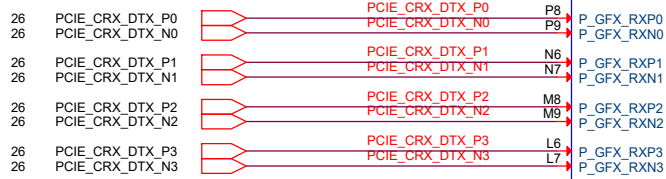
power plane State	V20B+ +3VL +5VLP	+5VALW +3VALW (+3VALW APU) +1.8VALW +0.9VALW	+1.2V	+5VS +3VS +1.8VS +0.9VS +0.6VS +2.5VS +VDDC_VDD +VDDCR_SOC
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

Port List

[illegible][illegible]

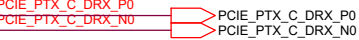
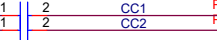
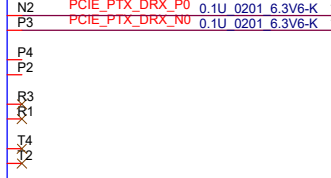
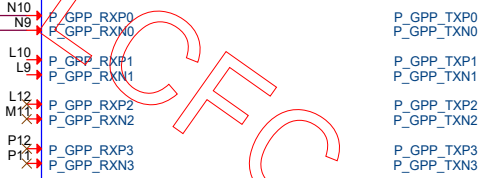
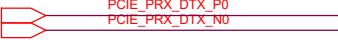
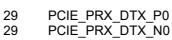
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Issued Date	2013/08/15	Deciphered Date	2013/08/15	
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Friday, March 28, 2018 IS 2 af 40				

M.2 SSD1



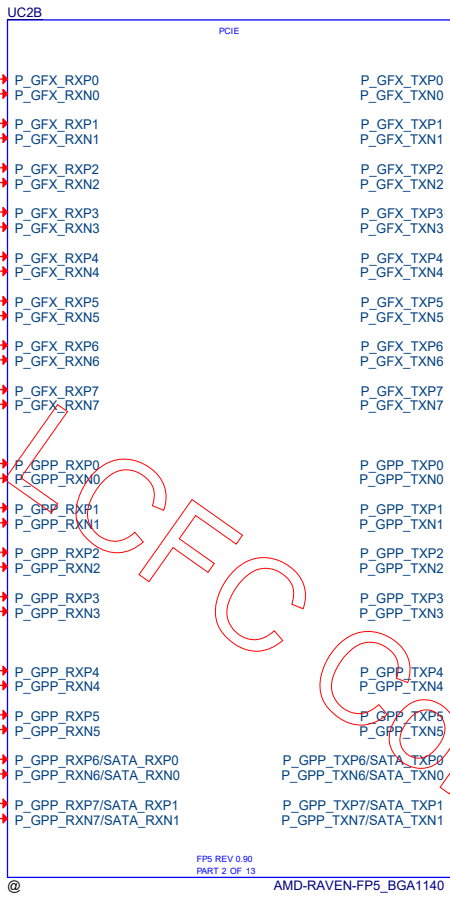
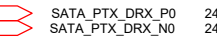
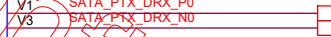
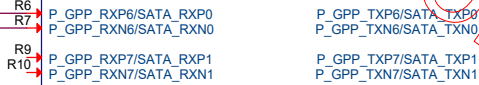
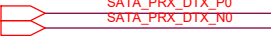
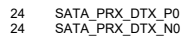
M.2 SSD1

WLAN



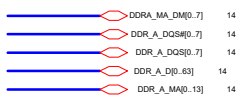
WLAN

SATA

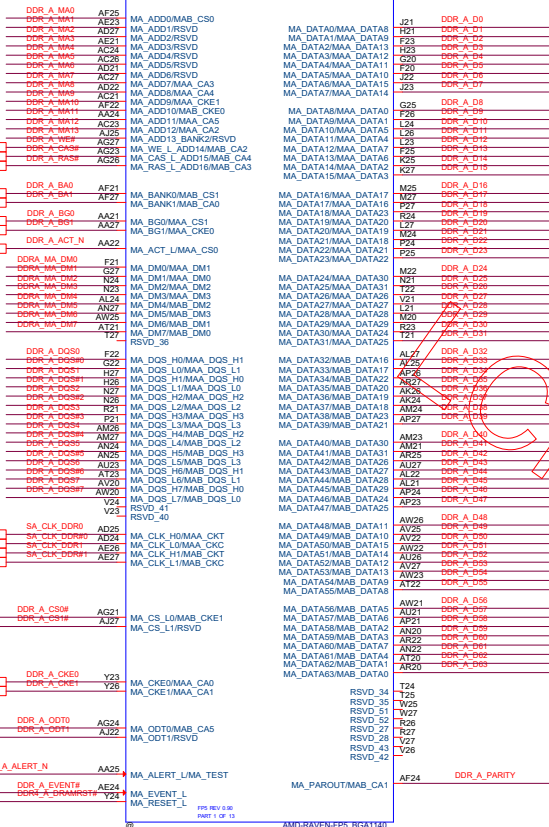


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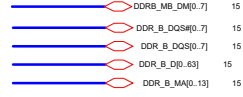
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FP5 (PCIE SATA I/F)		1.0	
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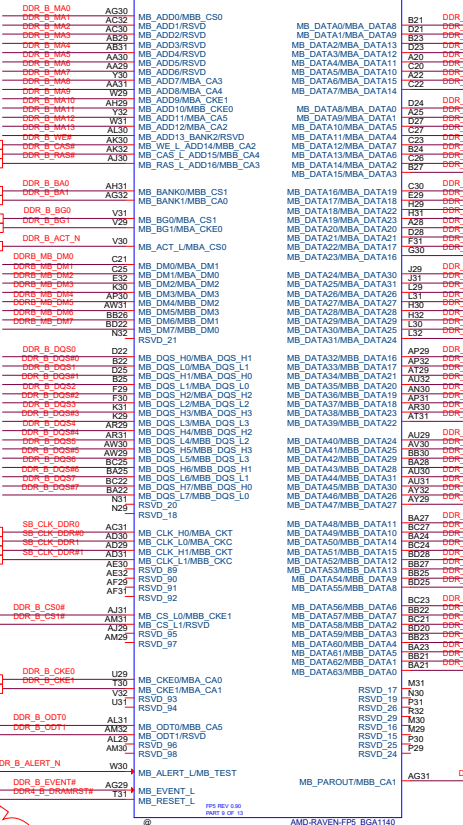
UC2A



SO-DIMM1



UC2I

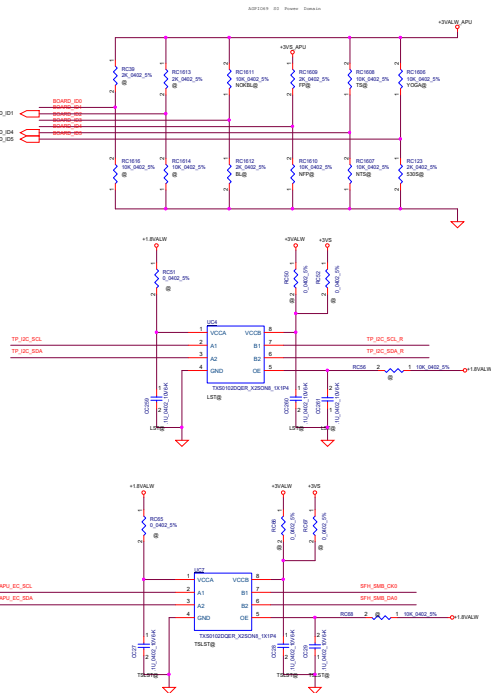


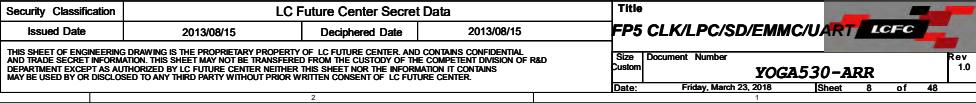
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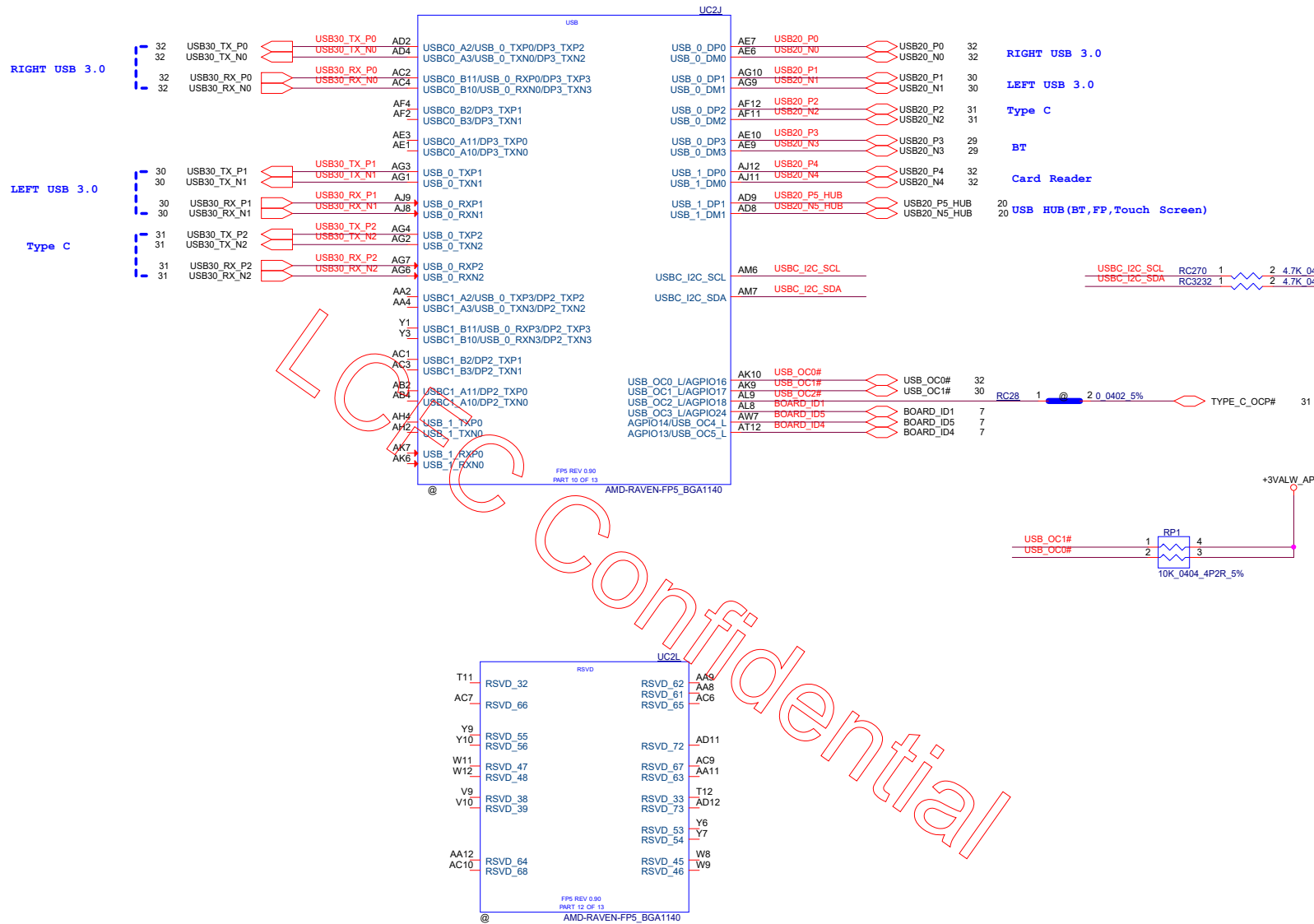
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Board ID	Description	Stuff #
Board_ID0	0	Reserved
Board_ID1	1	Reserved
Board_ID2	0	SATA SSD
Board_ID3	1	SSD-K8L
Board_ID4	0	SSD-K8L
Board_ID5	1	SSD-K8L
Board_ID6	0	SSD-K8L
Board_ID7	1	SSD-K8L
Board_ID8	0	SSD-K8L
Board_ID9	1	SSD-K8L
Board_ID10	0	SSD-K8L
Board_ID11	1	SSD-K8L
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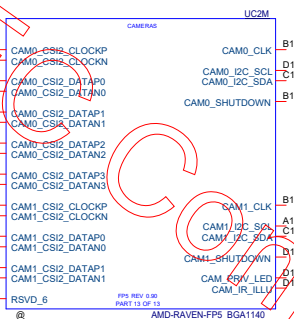
Project	2020-VDD 18.55	2020-VDD 18.55	2020-VDD 18.55	2020-VDD 18.55
VDD18.55 ARR	Touch Screen	Touch Pad	SO-DIMM2 / WLAN	EC Sensor Hub
VDD18.55 ARR	N/A	N/A	Cypress CCG4/Remanent	Touch Pad
ECES	N/A	N/A	SO-DIMM2	Touch Pad



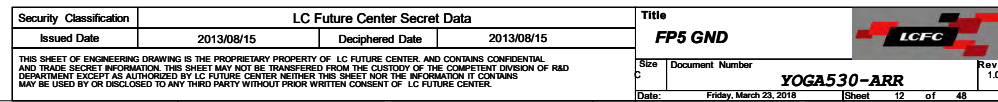


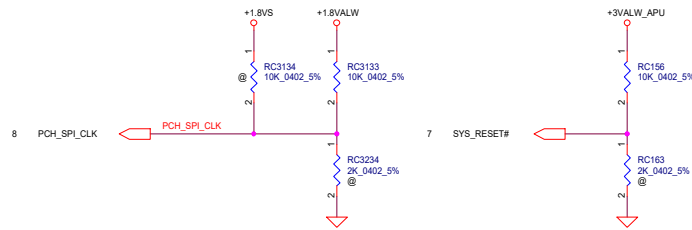


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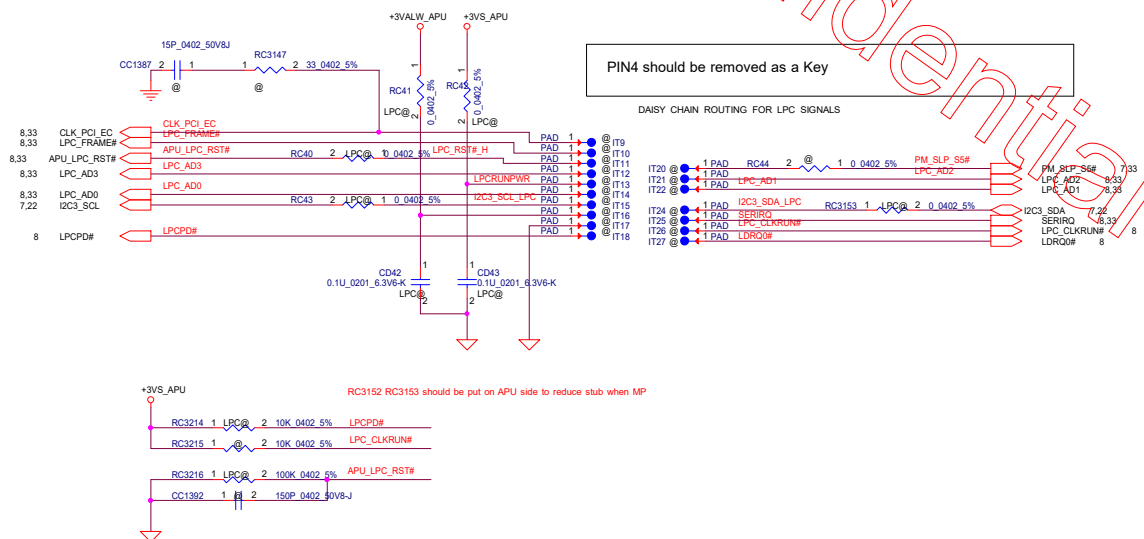
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STRAP PINS	SYS_RESET#
PCH_SPL_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE (DEFAULT) 0:SHORT RESET MODE

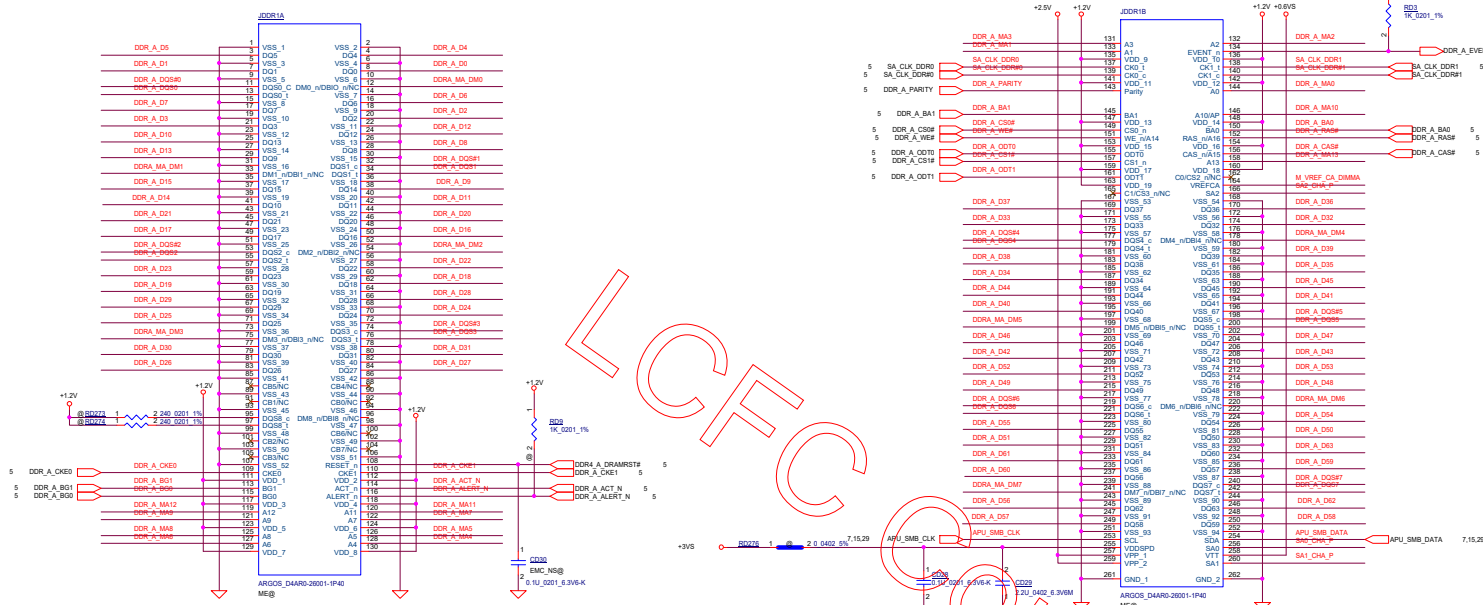
LPC ROM EMULATOR HEADER



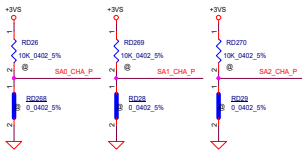


Swap Table

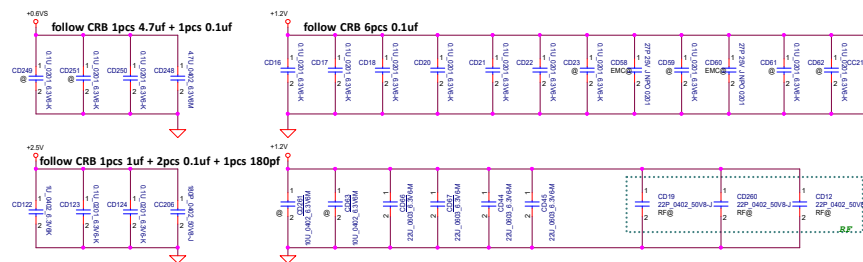
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DQ1	DDRA_DQ5
DQ2	DDRA_DQ4
DQ3	DDRA_DQ3
DQ4	DDRA_DQ2
DQ5	DDRA_DQ1
DQ6	DDRA_DQ0
DQ7	DDRA_DQ8#0
DQ8#0	DDRA_DQ8#0
DQ8#0	DDRA_DQ8#0
DQ8	DDRA_DQ12
DQ9	DDRA_DQ11
DQ10	DDRA_DQ10
DQ11	DDRA_DQ9
DQ12	DDRA_DQ8
DQ13	DDRA_DQ7
DQ14	DDRA_DQ6
DQ15	DDRA_DQ5
DQ16	DDRA_DQ4
DQ17	DDRA_DQ3
DQ18	DDRA_DQ2
DQ19	DDRA_DQ1
DQ20	DDRA_DQ0
DQ21	DDRA_DQ8#1
DQ22	DDRA_DQ8#1
DQ23	DDRA_DQ8#1
DQ24	DDRA_DQ8#1
DQ25	DDRA_DQ8#1
DQ26	DDRA_DQ8#1
DQ27	DDRA_DQ8#1
DQ28	DDRA_DQ8#1
DQ29	DDRA_DQ8#1
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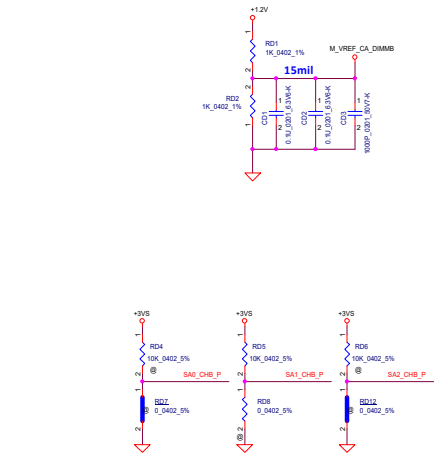
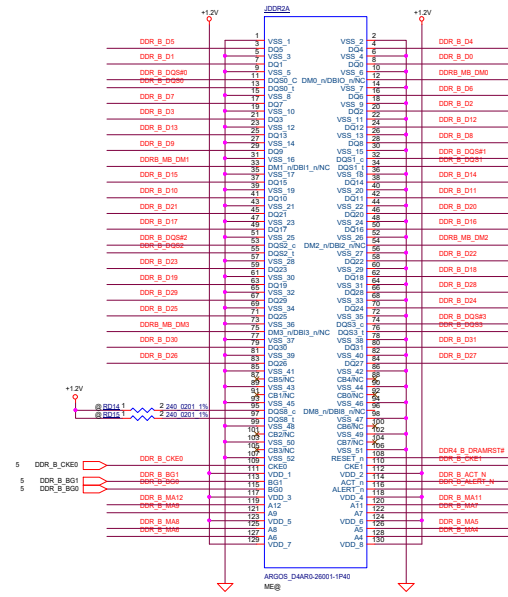


Layout Note: Place near JDDR1



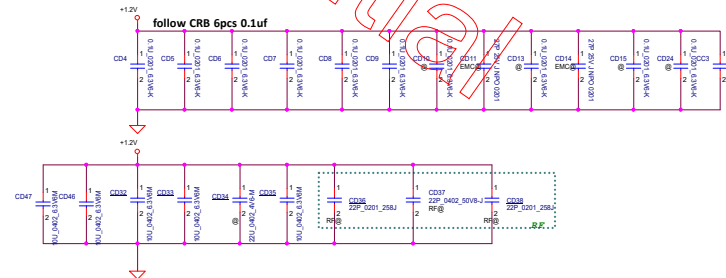
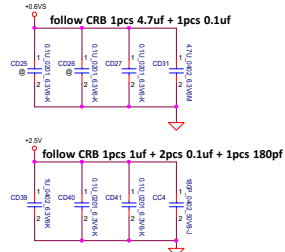
SPD Address = A0H





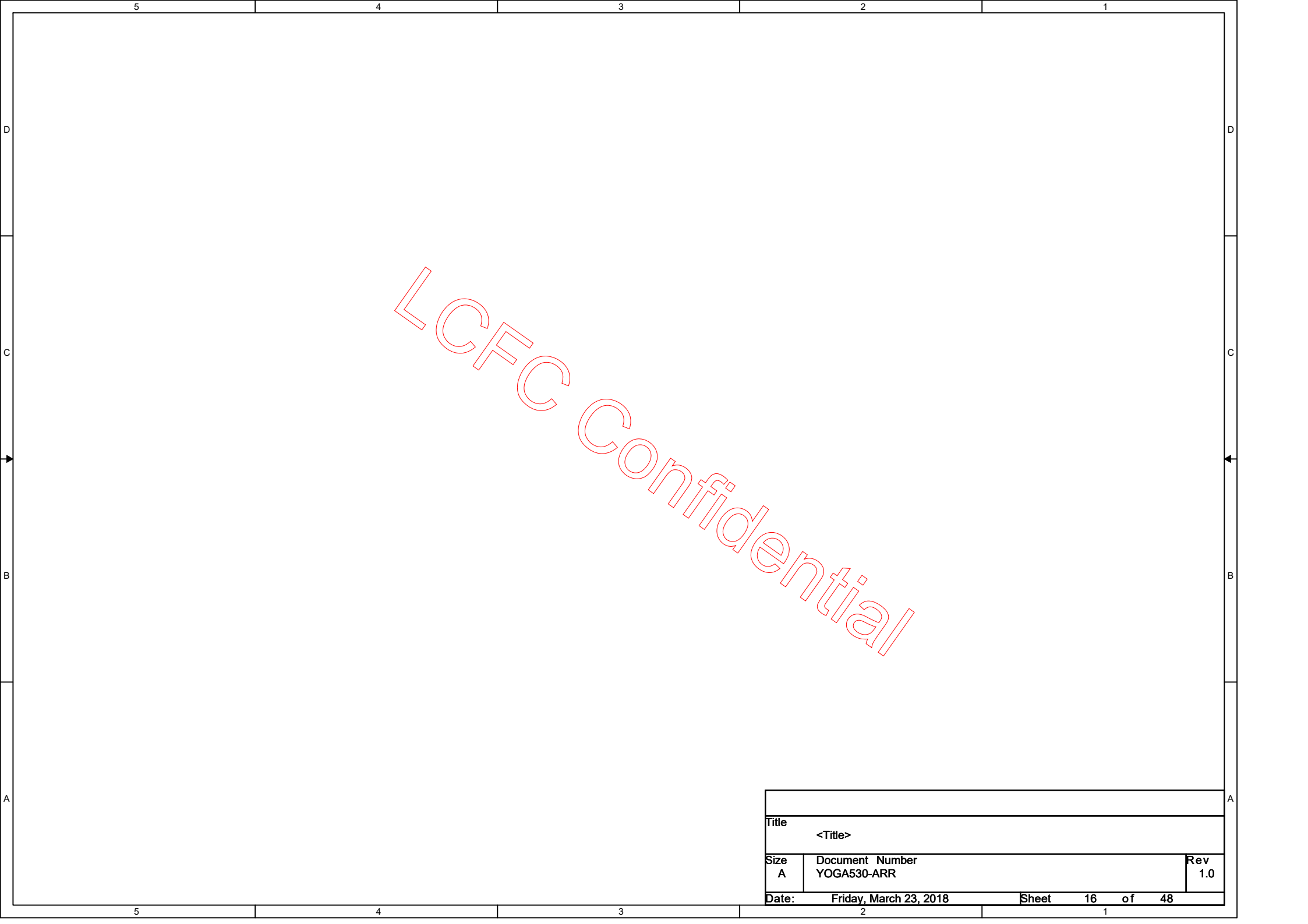
SPD Address = A4H

Layout Note: Place near JDDR2



Swap Table

Pin Name	Net Name
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DQ1	DQRA_DQ5
DQ2	DQRA_DQ4
DQ3	DQRA_DQ3
DQ4	DQRA_DQ2
DQ5	DQRA_DQ1
DQ6	DQRA_DQ0
DQ7	DQRA_DQ0
DQ8#0	DQRA_DQ8#0
DQ8#1	DQRA_DQ8#1
DQ8	DQRA_DQ12
DQ9	DQRA_DQ13
DQ10	DQRA_DQ14
DQ11	DQRA_DQ15
DQ12	DQRA_DQ9
DQ13	DQRA_DQ8
DQ14	DQRA_DQ15
DQ15	DQRA_DQ11
DQ8#1	DQRA_DQ8#1
DQ8#1	DQRA_DQ8#1
DQ16	DQRA_DQ20
DQ17	DQRA_DQ21
DQ18	DQRA_DQ22
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DQ22	DQRA_DQ23
DQ23	DQRA_DQ18
DQ24	DQRA_DQ2
DQ25	DQRA_DQ2
DQ26	DQRA_DQ21
DQ27	DQRA_DQ27
DQ28	DQRA_DQ28
DQ29	DQRA_DQ24
DQ30	DQRA_DQ26
DQ31	DQRA_DQ30
DQ8#3	DQRA_DQ8#3
DQ8#3	DQRA_DQ8#3
DQ32	DQRA_DQ37
DQ33	DQRA_DQ33
DQ34	DQRA_DQ34
DQ35	DQRA_DQ38
DQ36	DQRA_DQ32
DQ37	DQRA_DQ36
DQ38	DQRA_DQ35
DQ39	DQRA_DQ39
DQ40	DQRA_DQ34
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DQ42	DQRA_DQ47
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DQ8#7	DQRA_DQ8#7



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A	YOGA530-ARR		1.0
Date:	Friday, March 23, 2018	Sheet	16 of 48

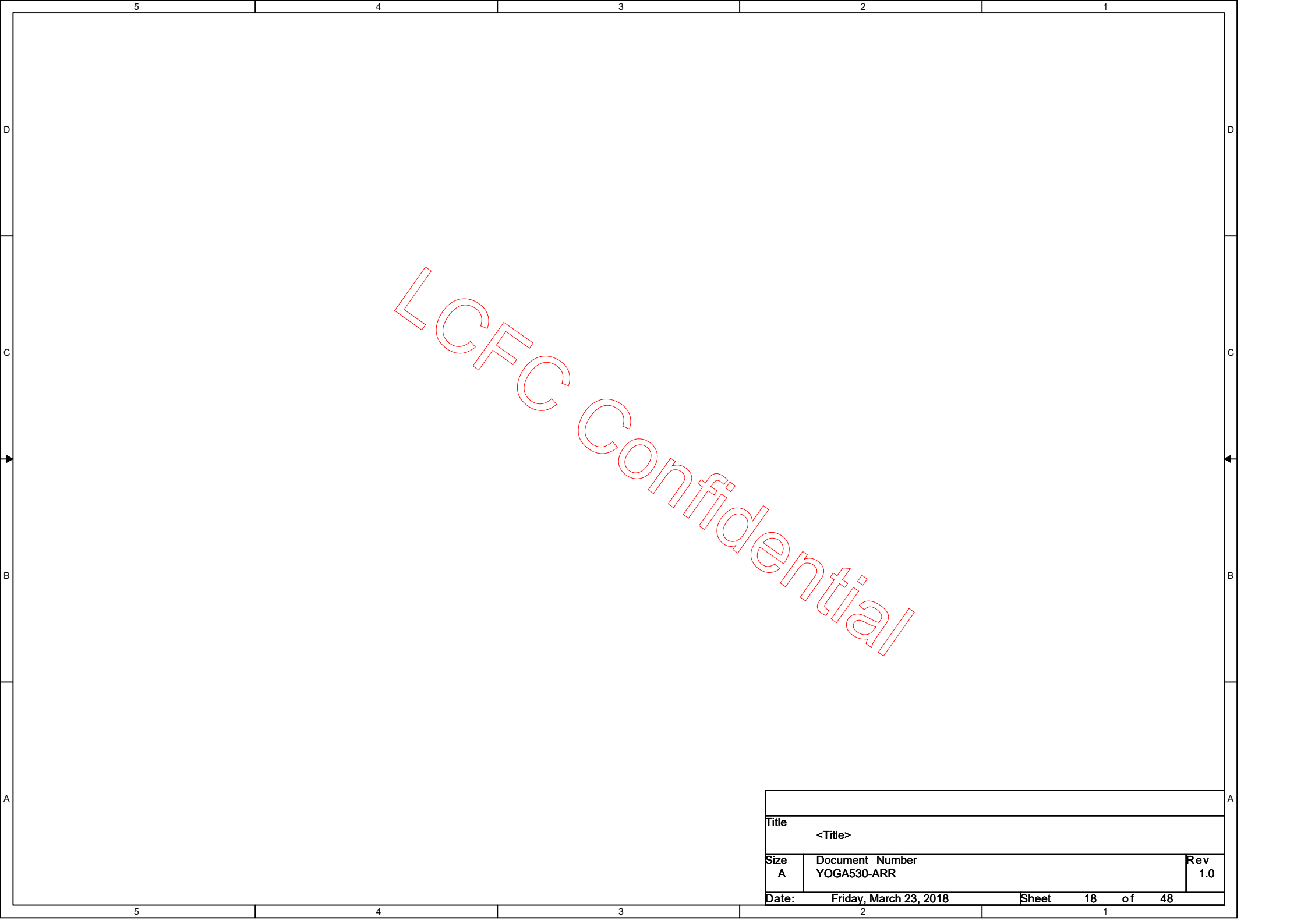
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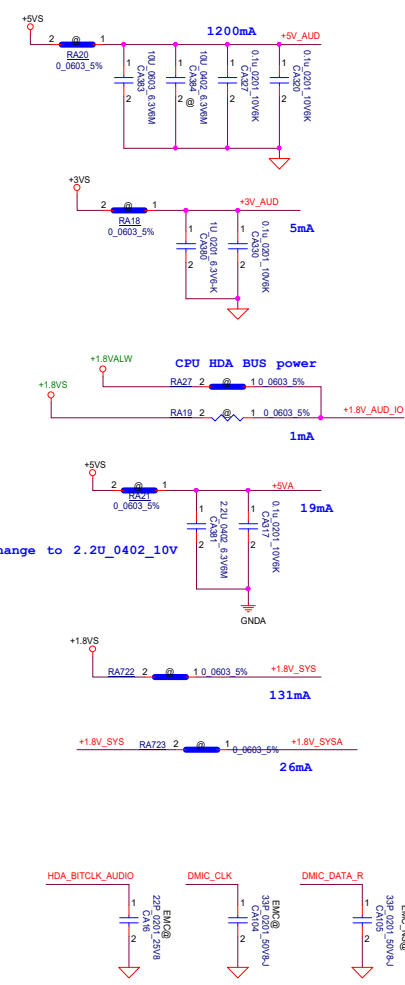
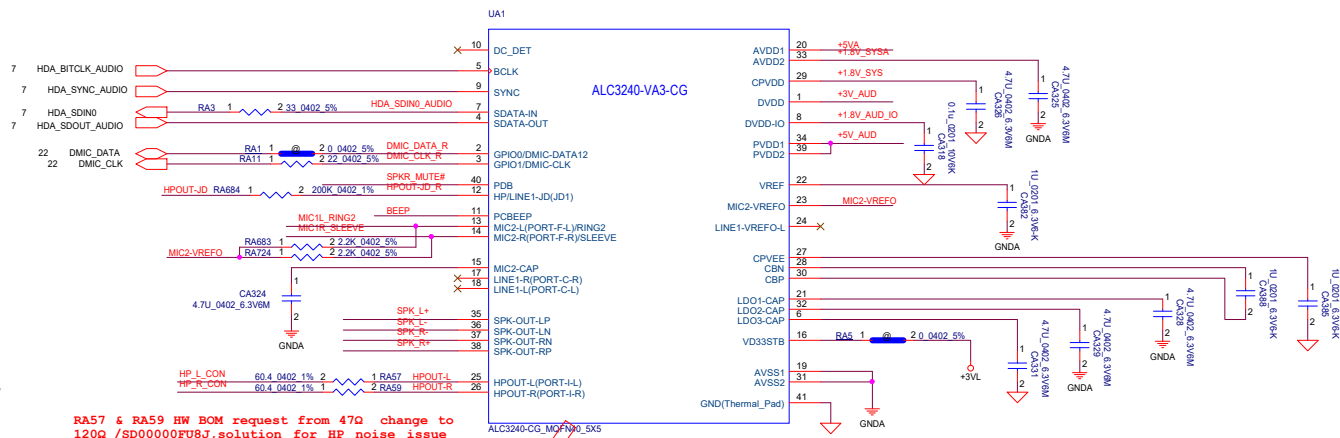
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Size A		Document Number YOGA530-ARR																				Rev 1.0		
Date:		Friday, March 23, 2018												Sheet		17		of		48				

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Title <Title>			
Size A	Document Number YOGA530-ARR		Rev 1.0
Date:	Friday, March 23, 2018	Sheet 17 of 48	





VD33STB:Power for combo jack depop circuit at system shutdown mode.

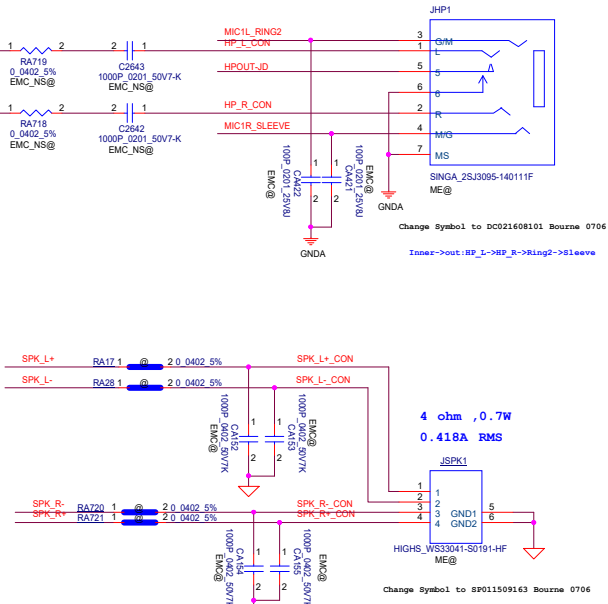
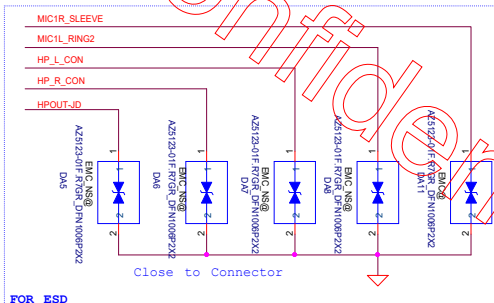
AVDD1:Analog power for mixers ,IO ports

DVDD-IO:Digital power for HDA link

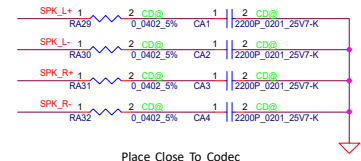
DVDD:Digital power for digital I/O circuit

AVDD2:Analog power for DACS ,ADCS

PVDD1,PVDD2:Power supply for full-bridge left and right channel

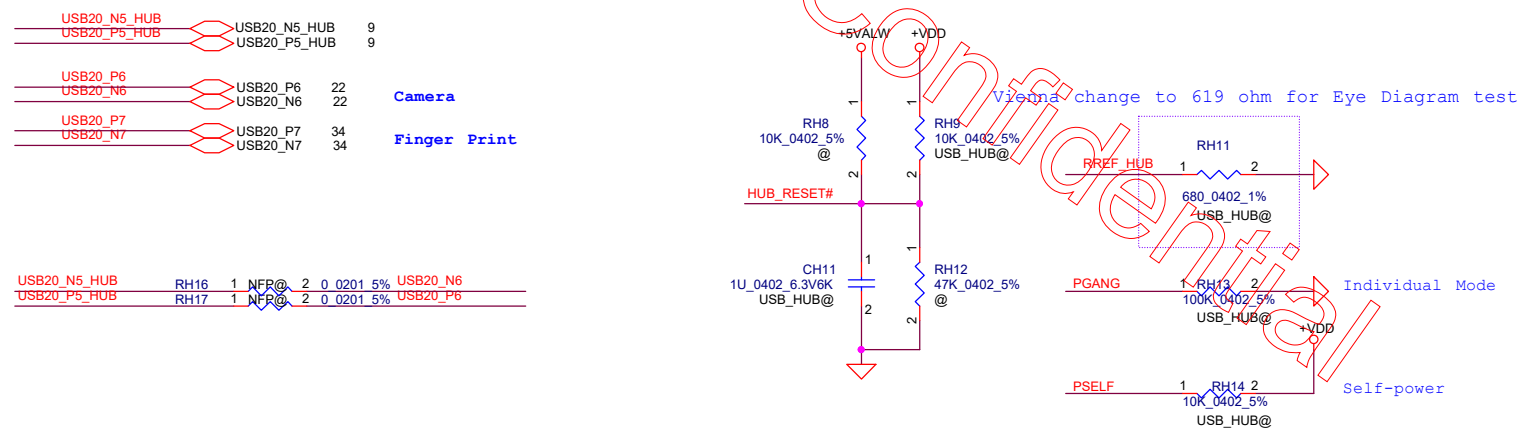
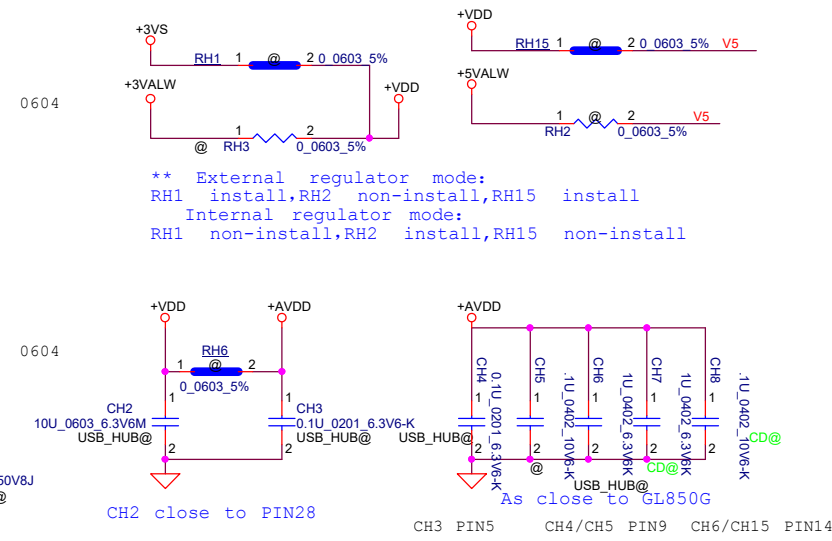
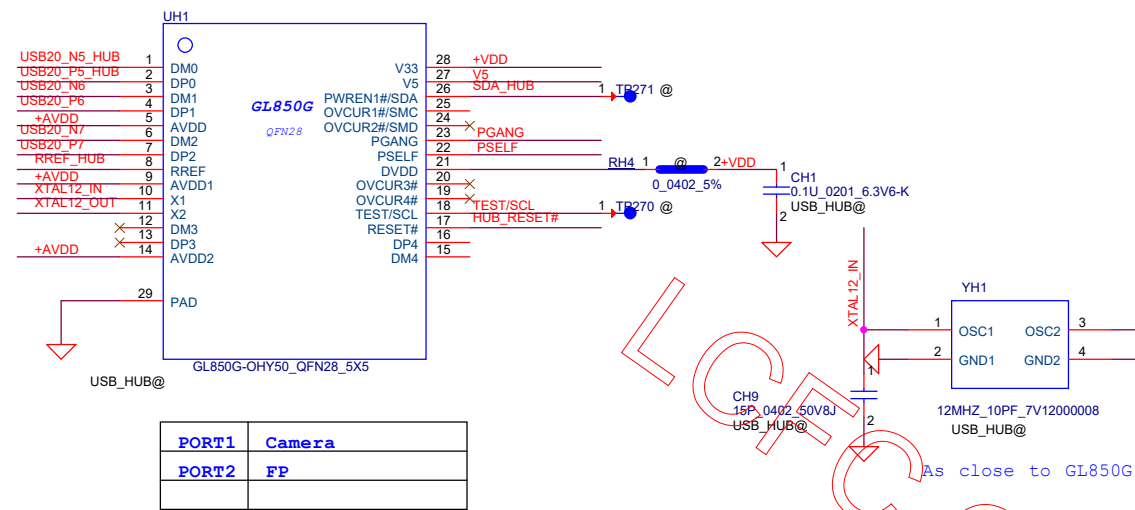


RA29,RA30,RA31,RA32 will be changed from 150ohm to 0ohm, for HW SO---->S3 play music hang up issue solution



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		Date:		Friday, March 23, 2018	Sheet 19 of 48

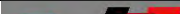
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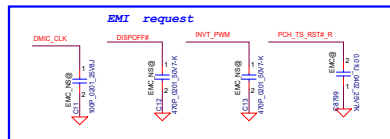
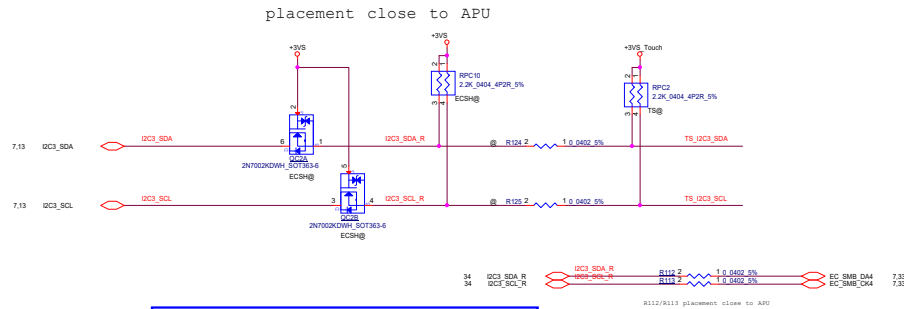
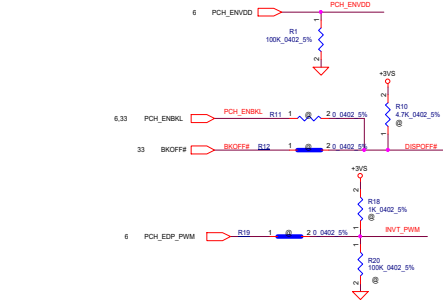
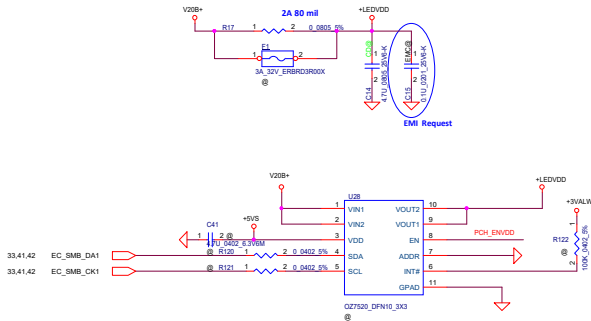
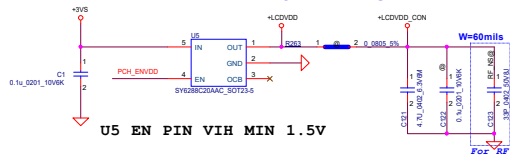
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				YOGA530-ARR	
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				Rev	1.0

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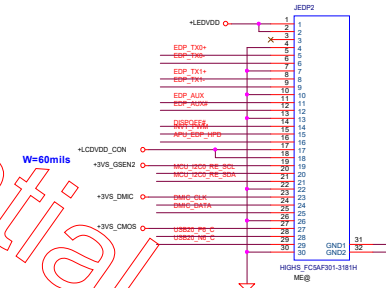
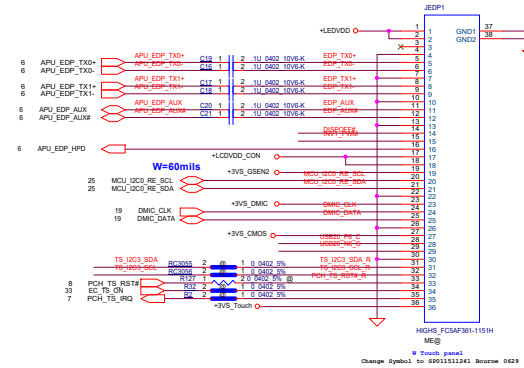
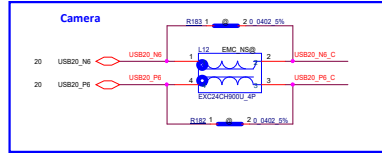
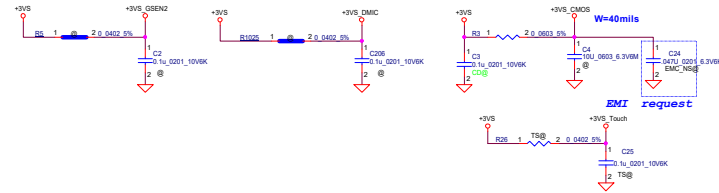
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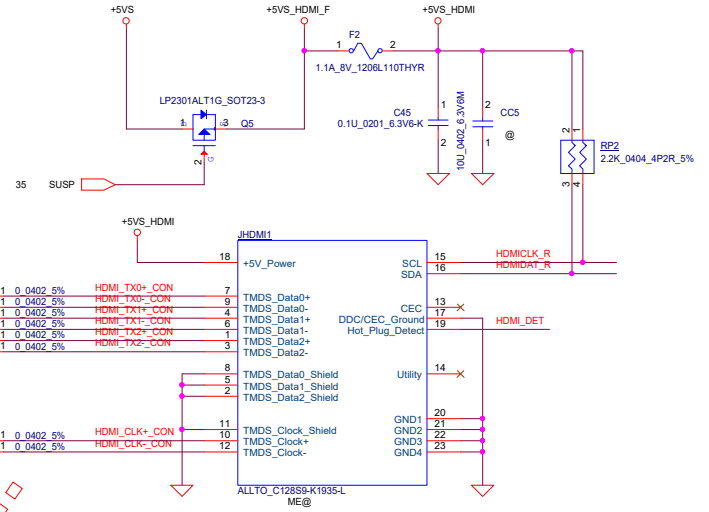
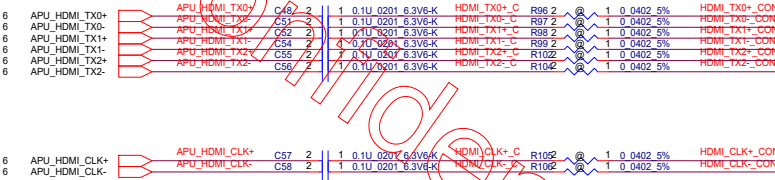
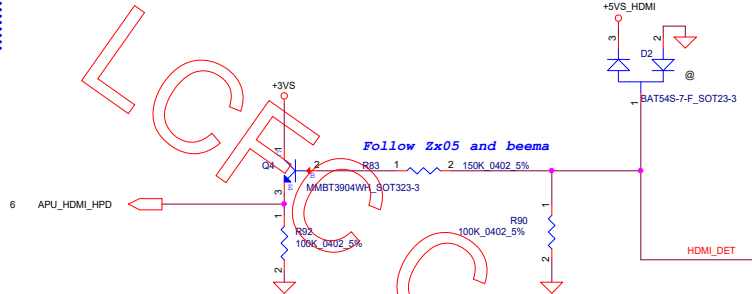
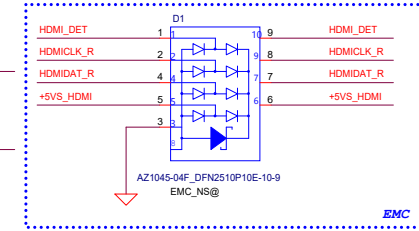
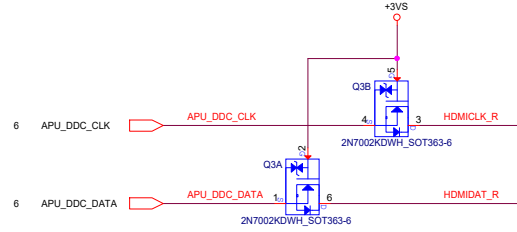
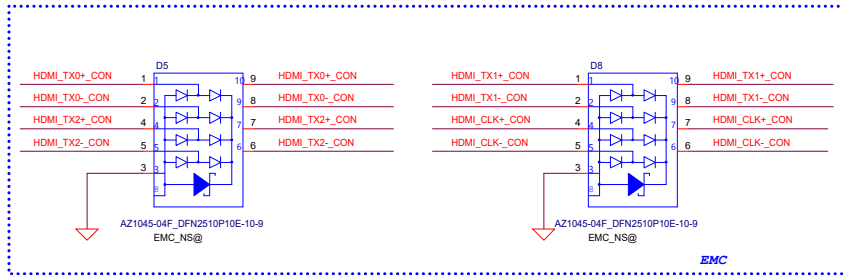
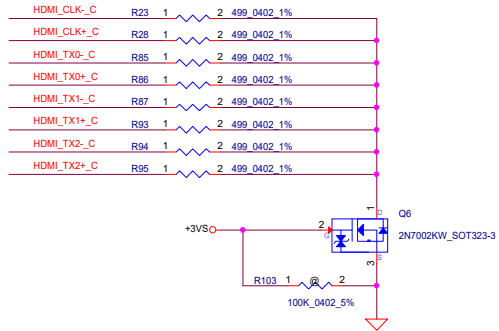
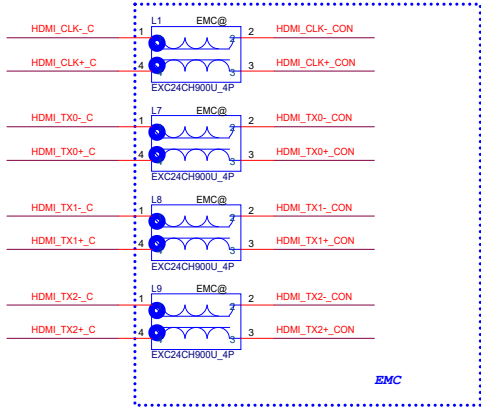
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LCD POWER CIRCUIT



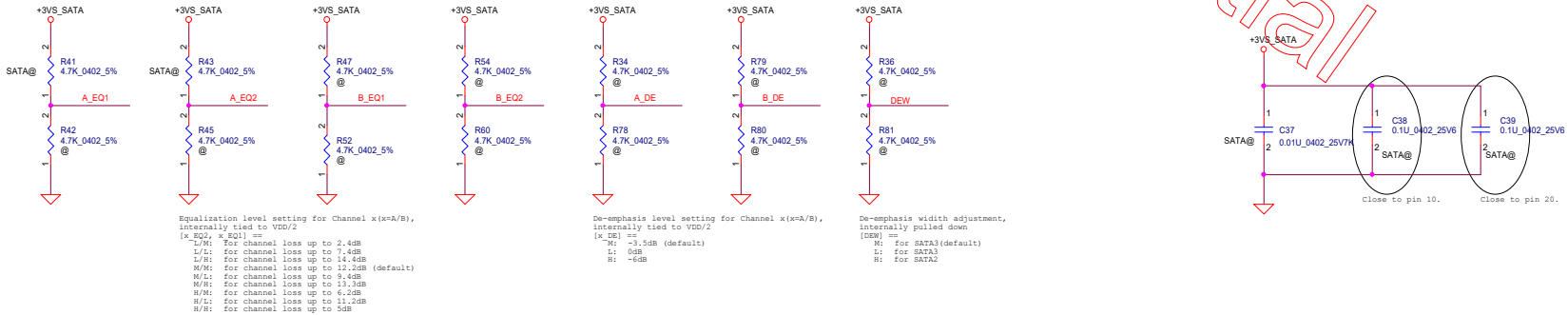
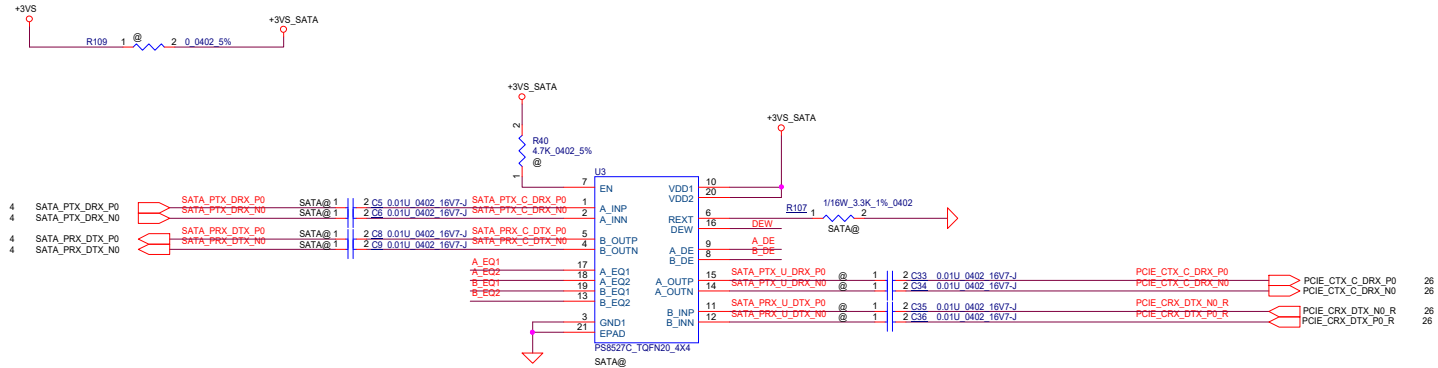
CMOS Camera





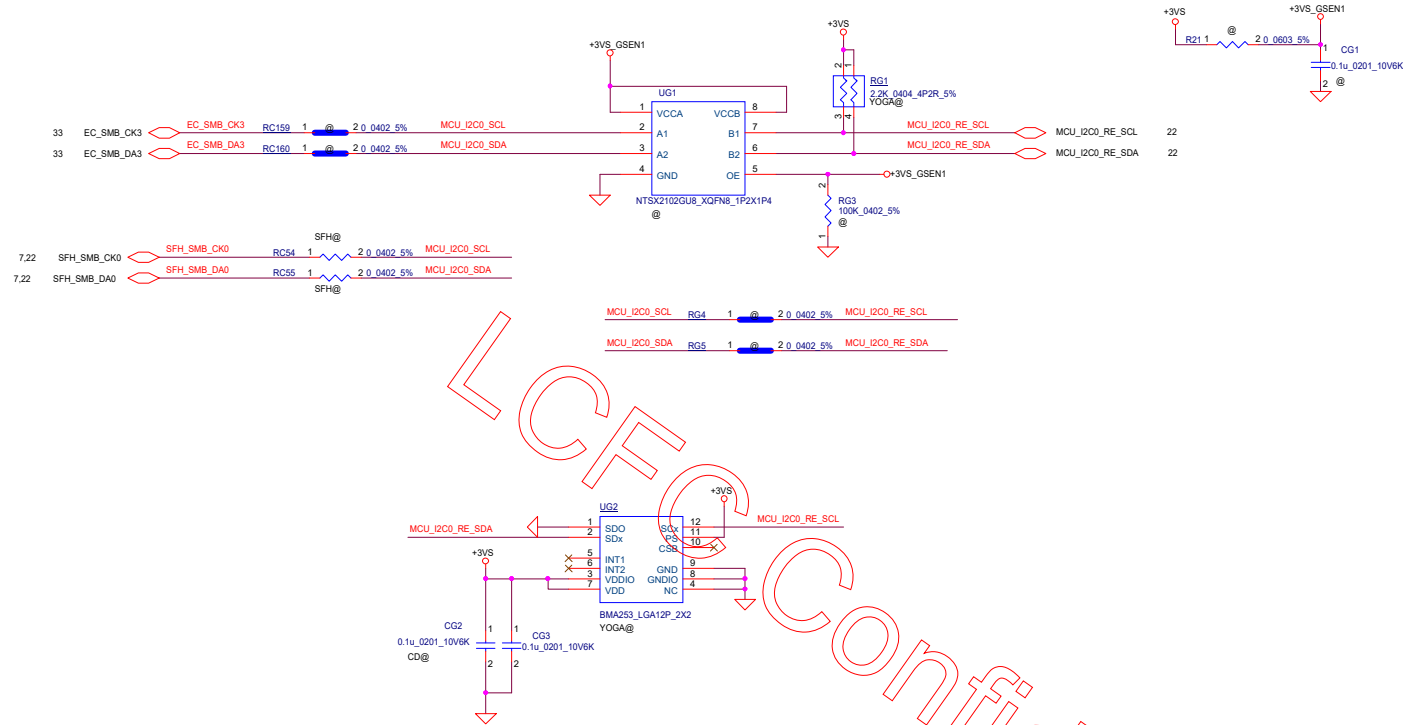
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						Custom		YOGA530-ARR	1.0
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SATA HDD Redriver

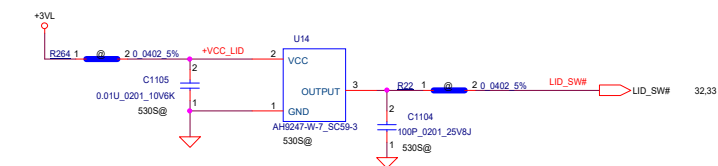


Follow Vendor suggest

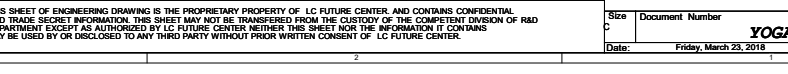
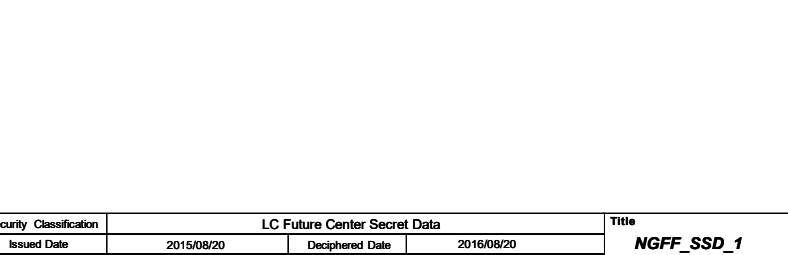
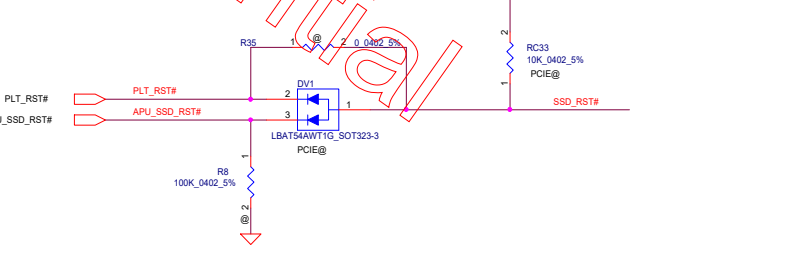
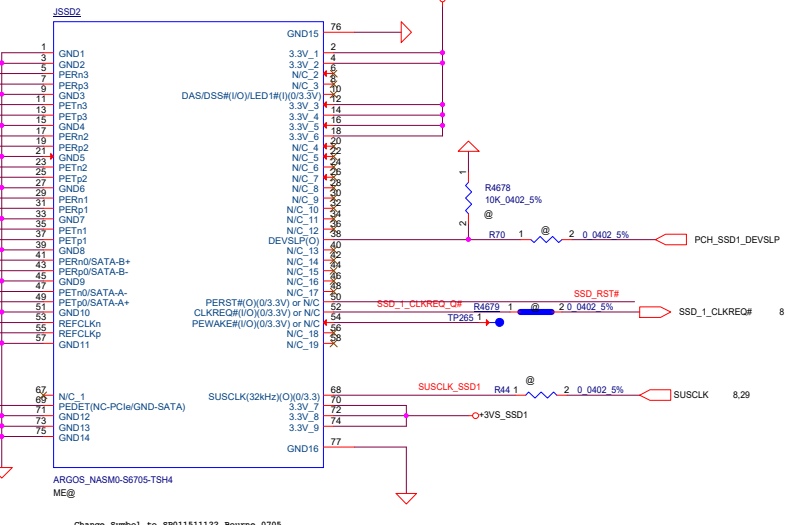
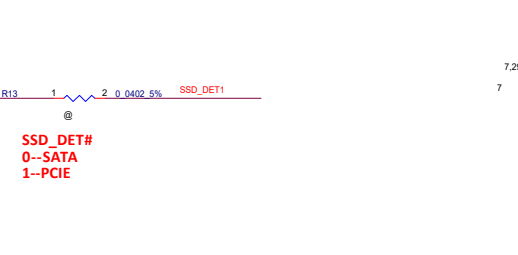
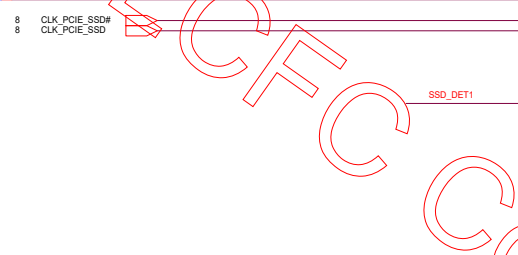
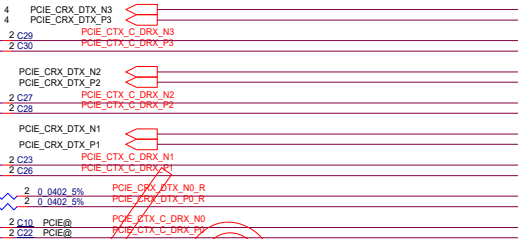
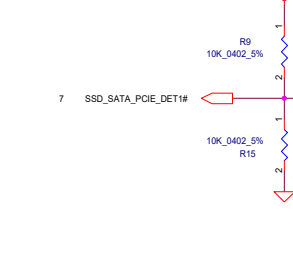
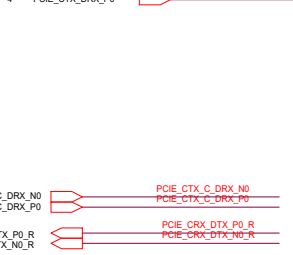
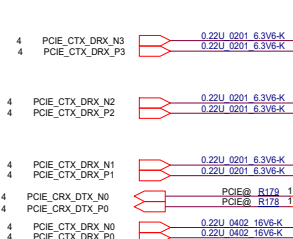
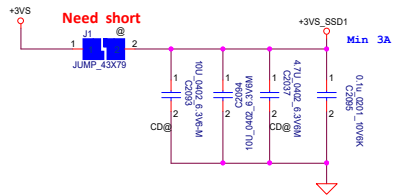
G-SENSOR



LID switch



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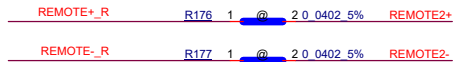


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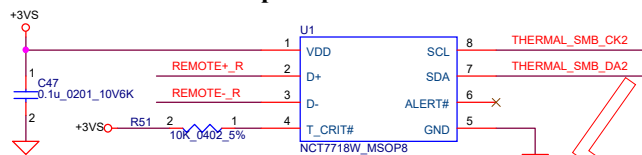
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Close to U1

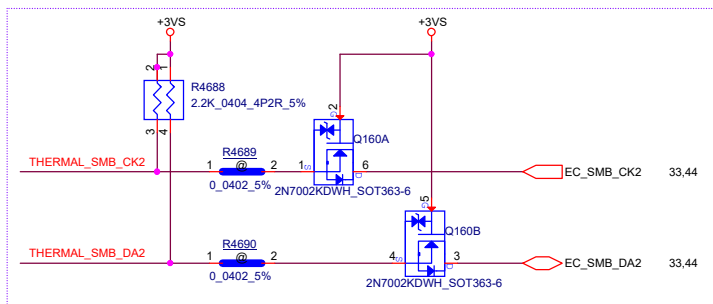


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Trace length:<8"

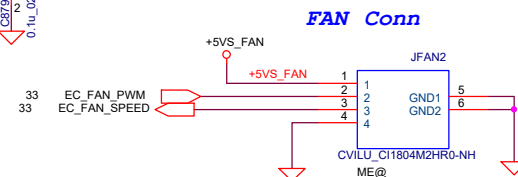
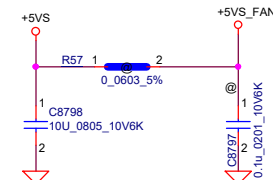
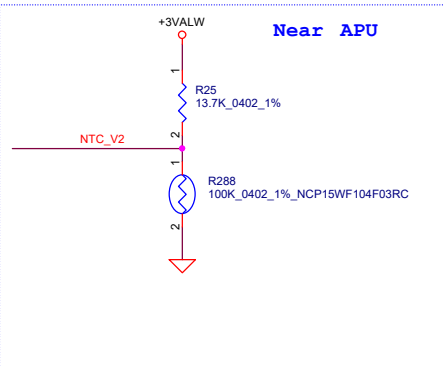
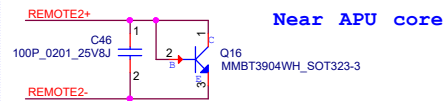
SMSC thermal sensor
placed near DIMM



Address 1001_101xb



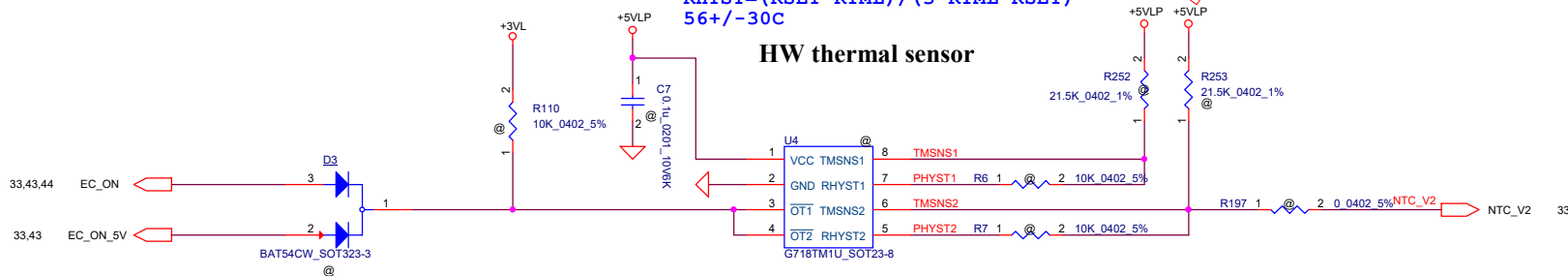
Near GPU&VRAM



Change Symbol to SP01001J000 Bourne 0629

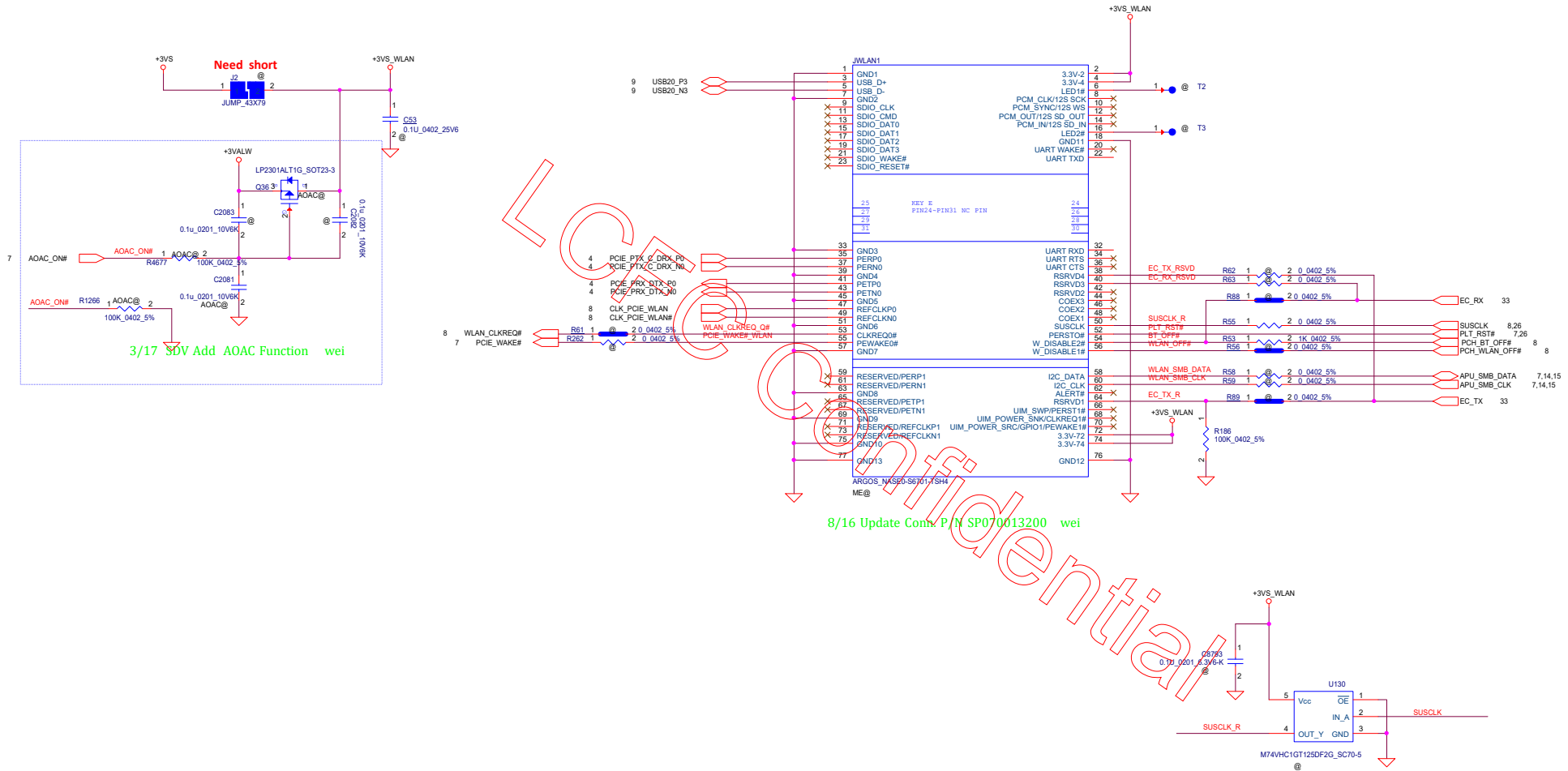
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST= (RSET*RTML) / (3*RTML-RSET)
56+/-30C

HW thermal sensor



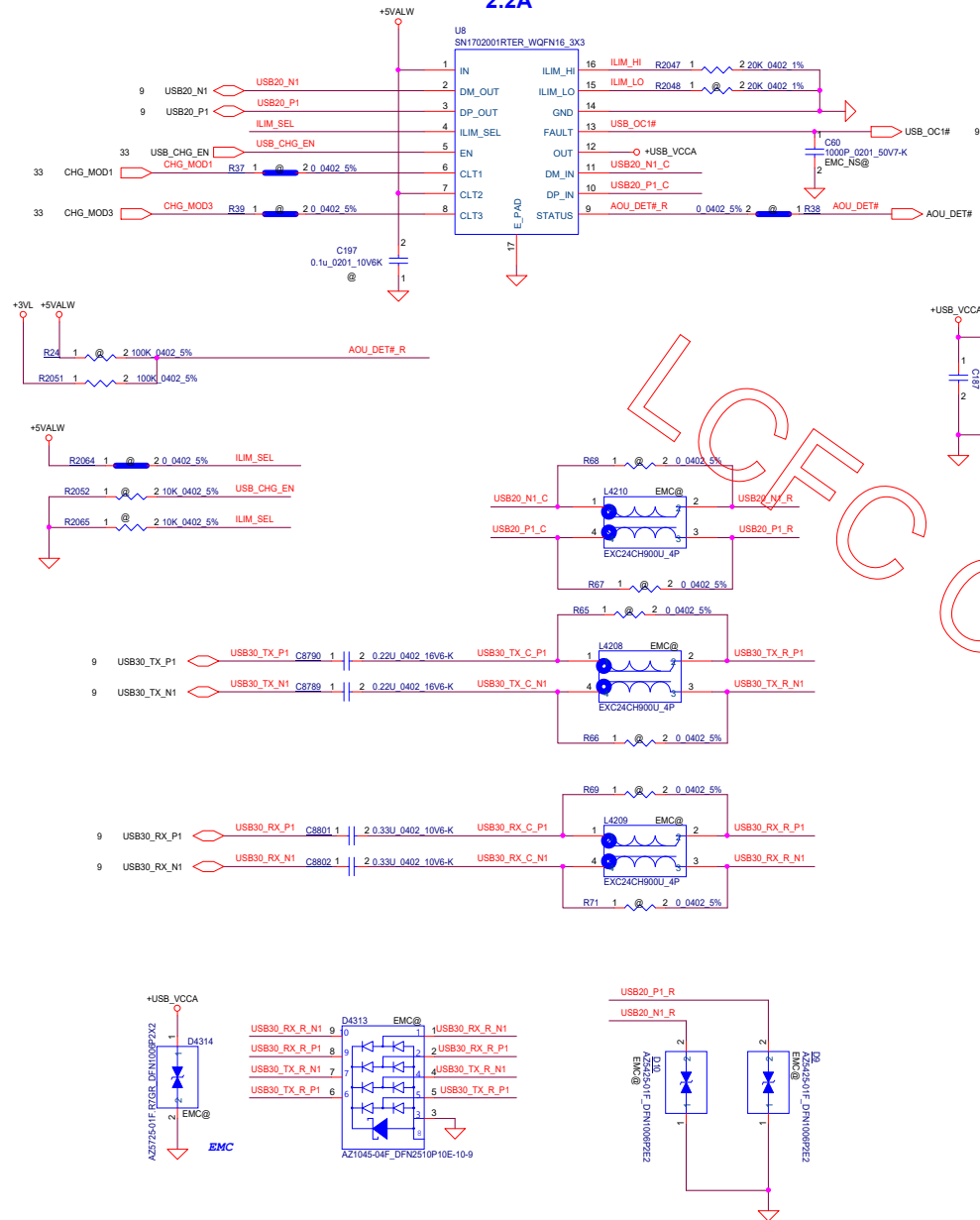
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Mini-Express Card(WLAN/WiMAX)

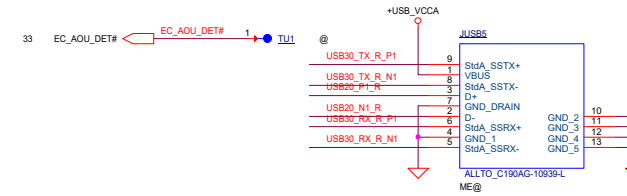


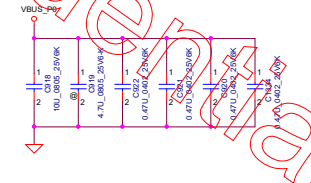
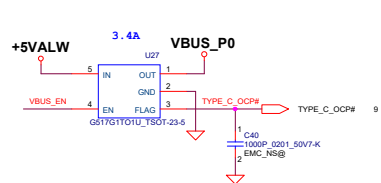
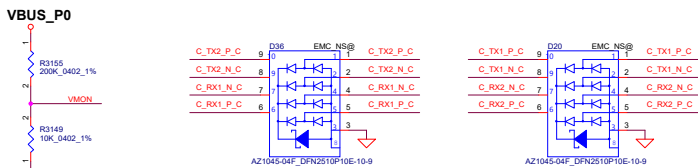
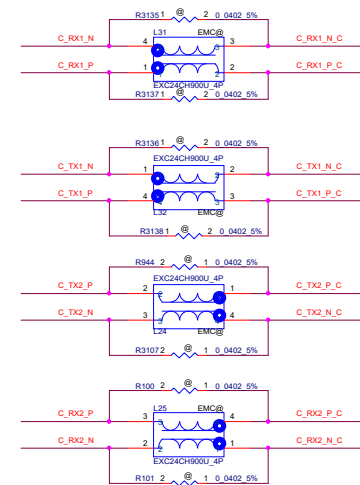
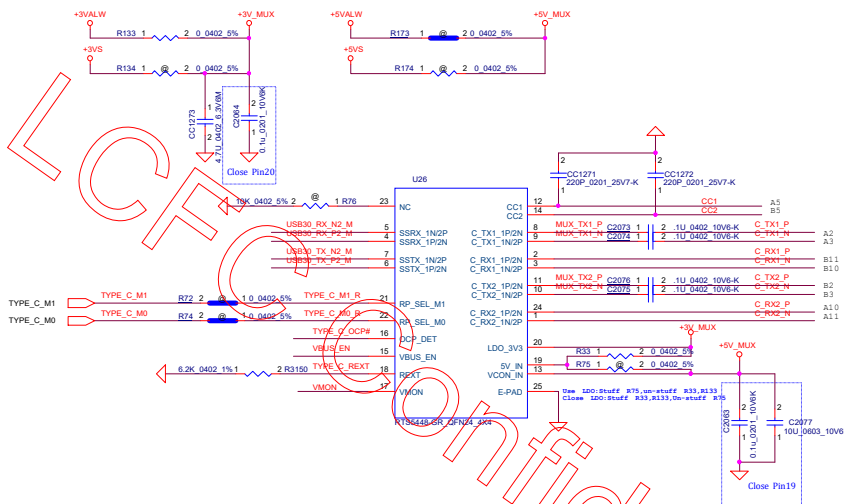
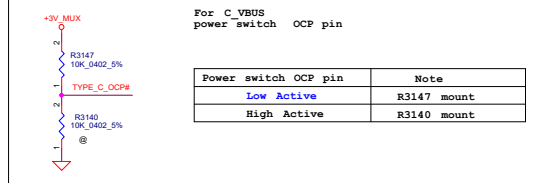
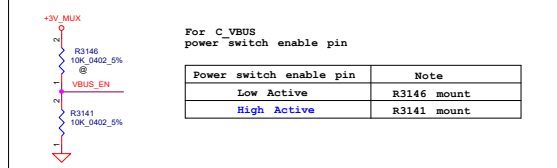
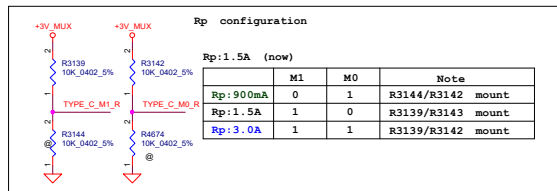
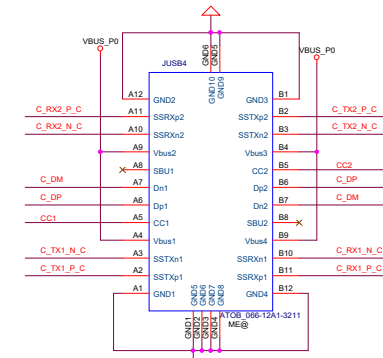
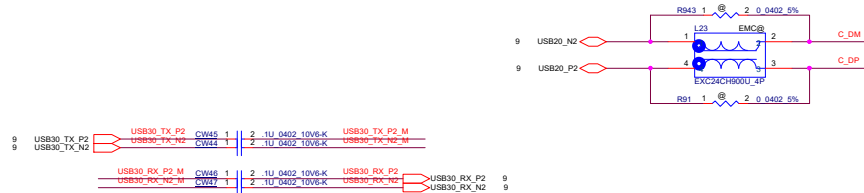
LEFT SIDE USB3.0 PORT x1

USB charger
2.2A



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1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active





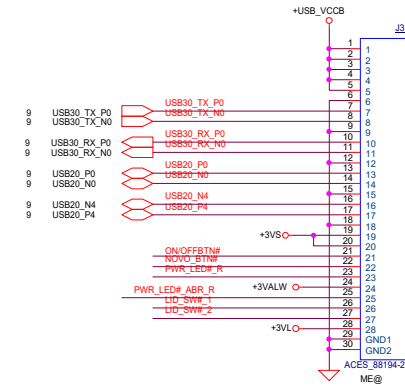
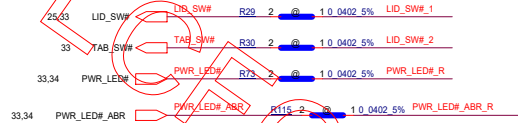
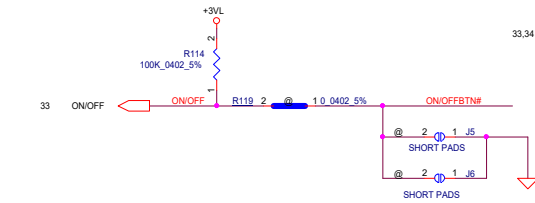
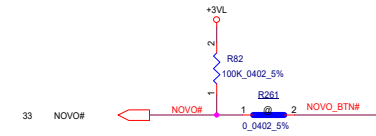
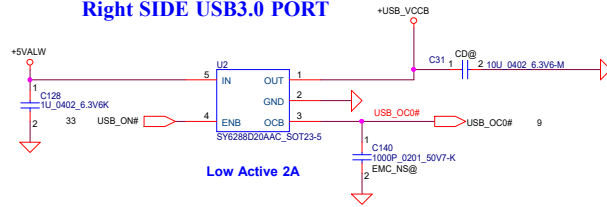
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Issued Date		2015/08/20		Deciphered Date	
				2016/08/20	
				TYPE-C_RTSS5448	
				Rev	
				1.0	
				Date	
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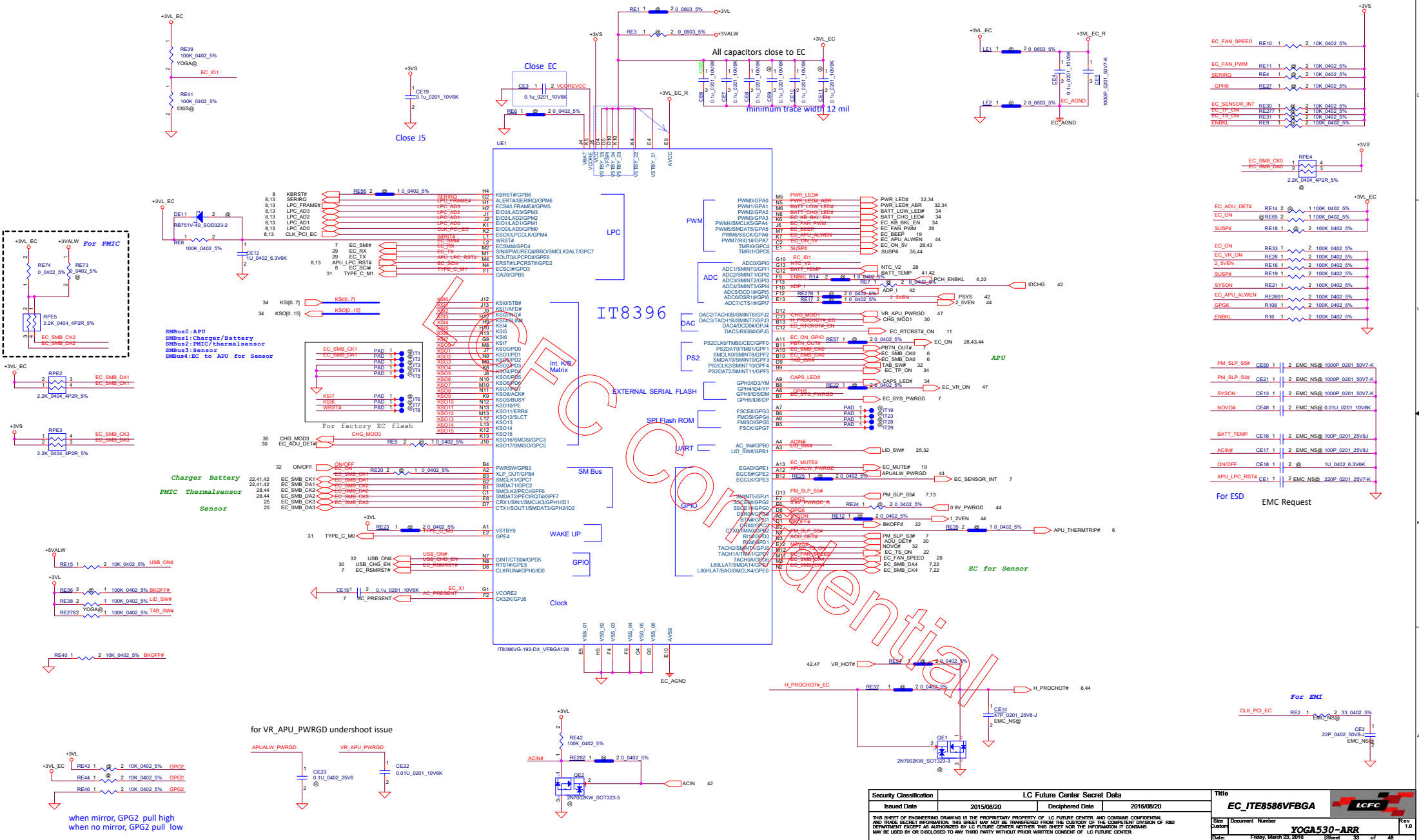


YOGA530-ARR

Right SIDE USB3.0 PORT



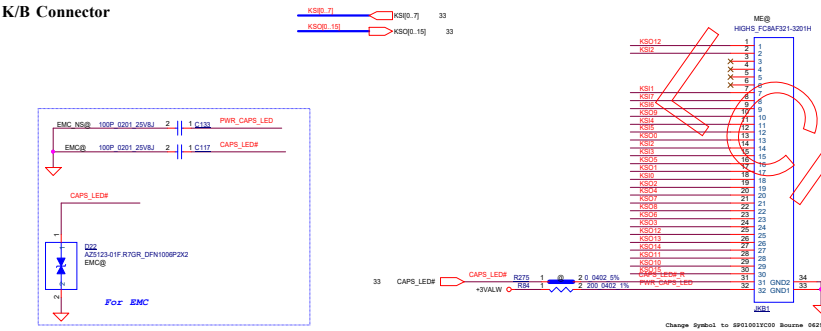
Confidential



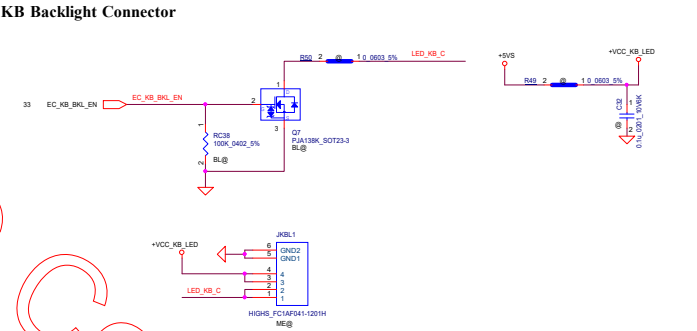
when mirror, GPG2 pull high
when no mirror, GPG2 pull low

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2015/08/20		2016/08/20			
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Revision		Document Number		YOGA530-ARR	
1.0					
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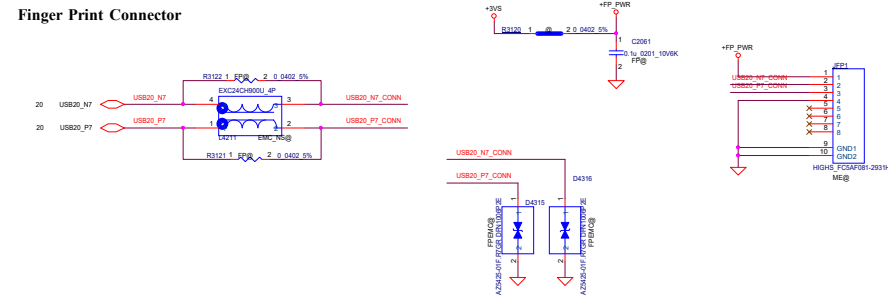
K/B Connector



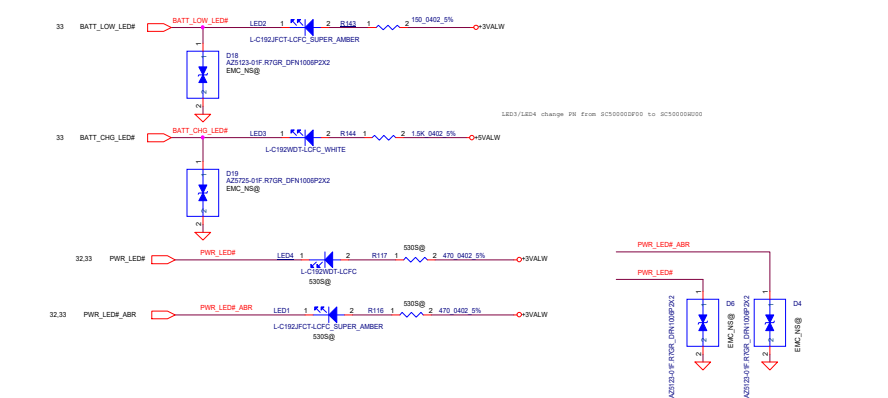
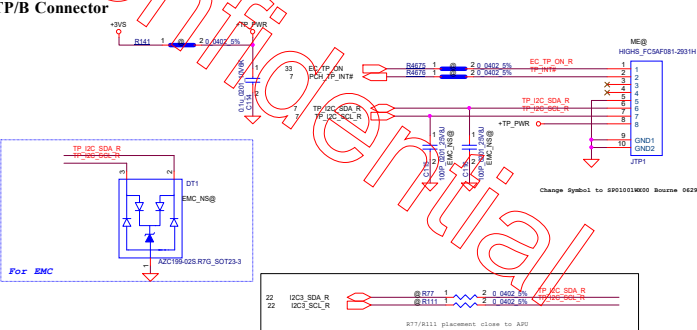
KB Backlight Connector



Finger Print Connector



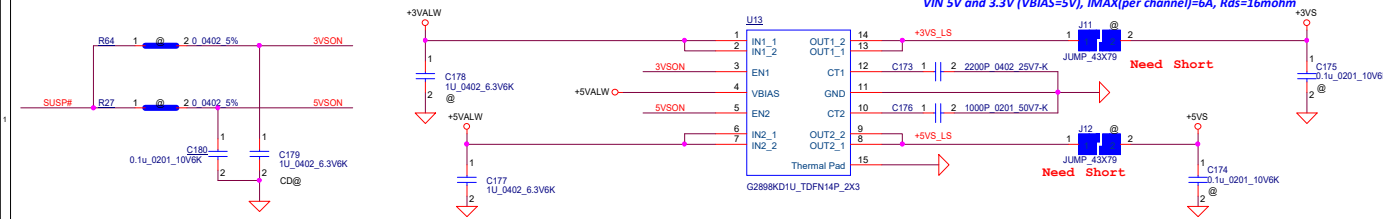
CP/B Connector



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				Rev 1.0	

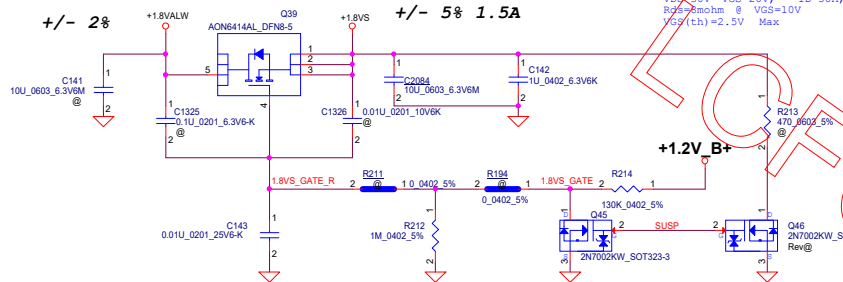
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



+1.8VALW to +1.8VS

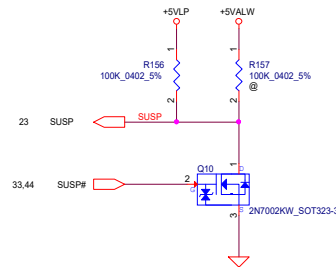
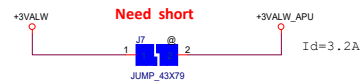
+/- 2%



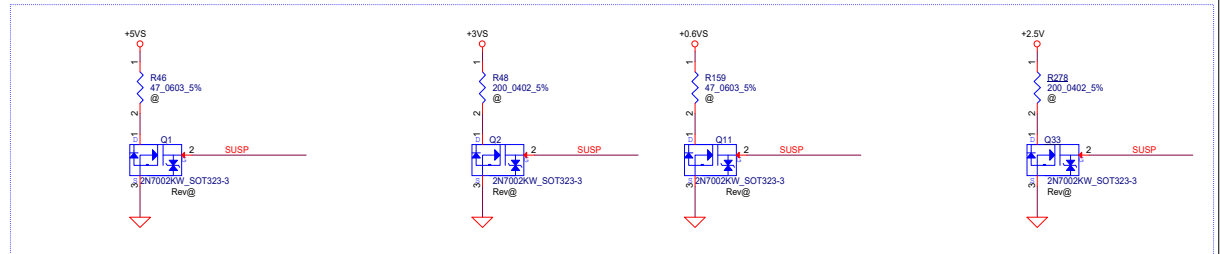
+/- 5% 1.5A
+1.2V_B+

+0.9V to +0.9VS

20VSB will change to 6V in DC mode, careful the Res divide voltage



For DisCharge



08/29: Need double check enable signal and the resistance

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ZZZ4

AMD Ryzen 7 2700U 2.2G/4C/6M/FP5
RT@
SA00008QB10

ZZZ2

AMD Ryzen 5 2500U 2.0G/4C/6M/FP5
RC@
SA00008QA10

ZZZ3

RAVEN RIDGE YM2500C4T4MFBA
R3@
SA00008JR10

APU type

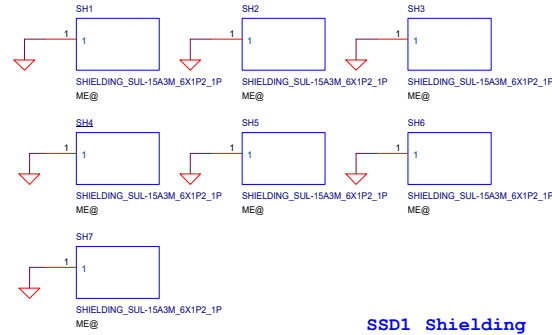
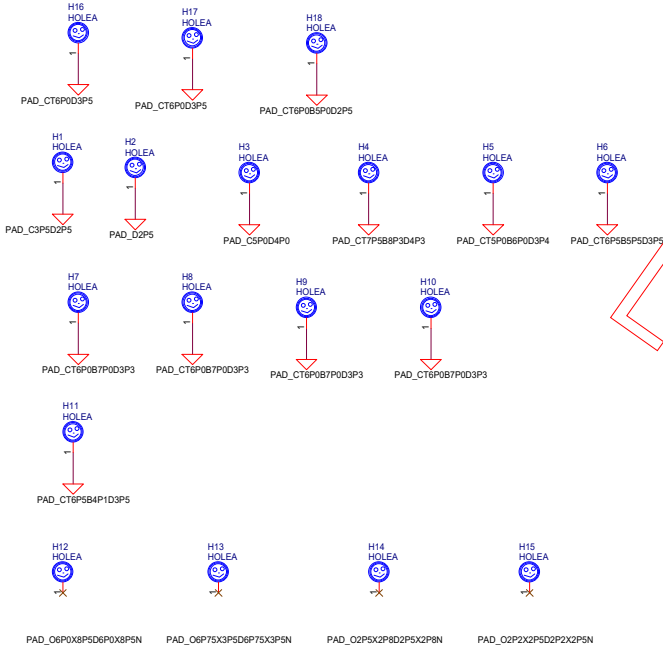
ZZZ1

NM-B781
DA800011R00
DA8@

PCB_MB

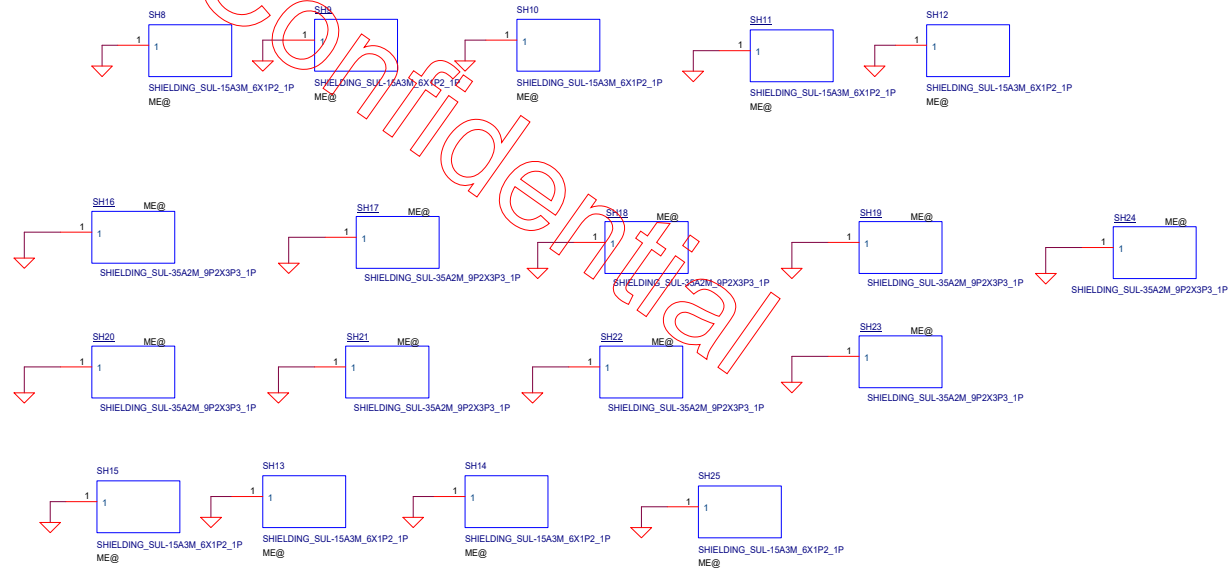
Hole

PCB Federal Mark PAD



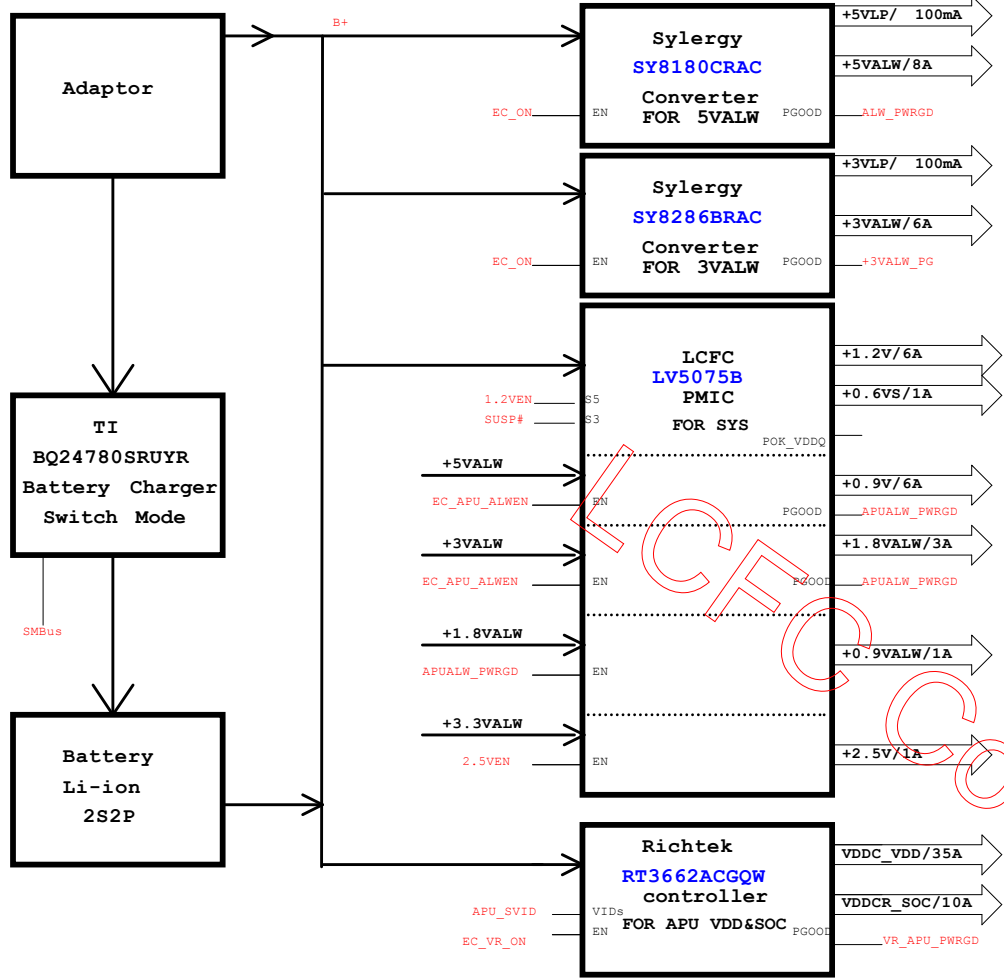
SSD1 Shielding

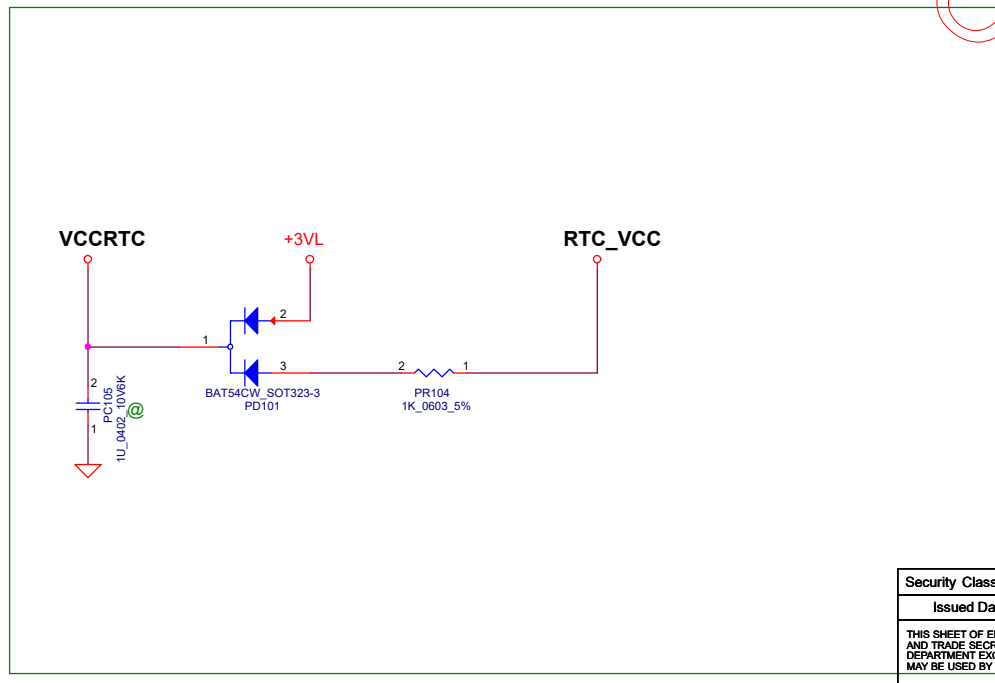
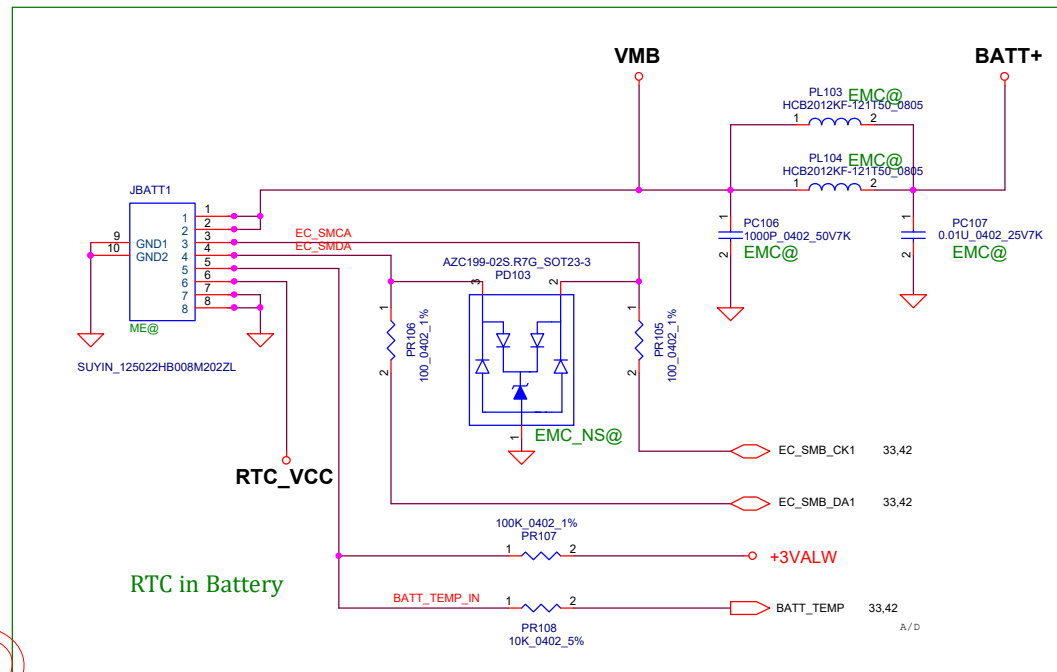
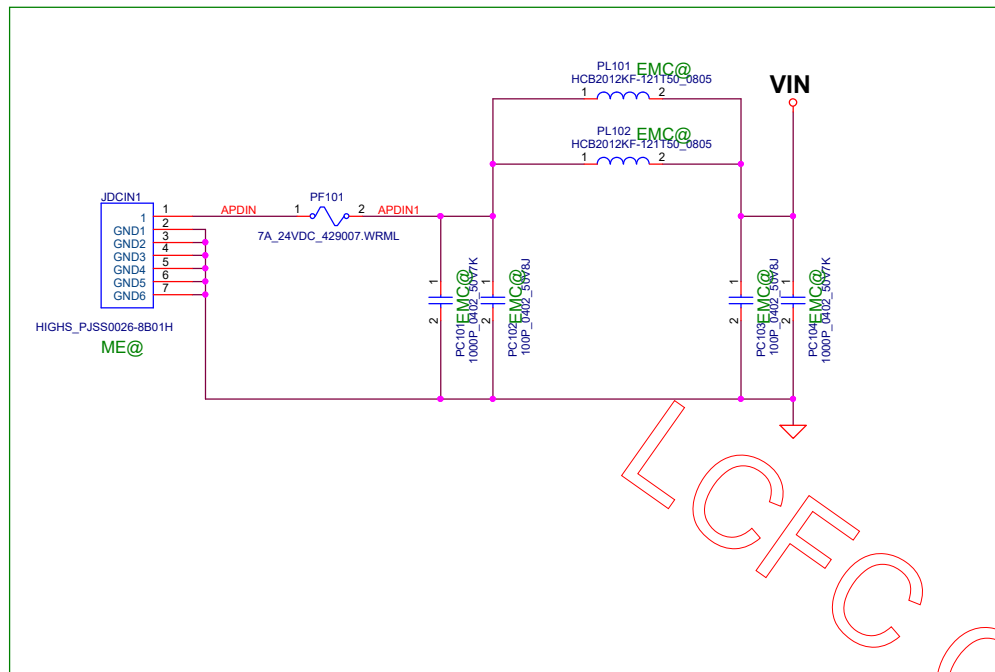
DDR Shielding



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2013/08/15		2013/08/15			
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				Sheet 39 of 48	

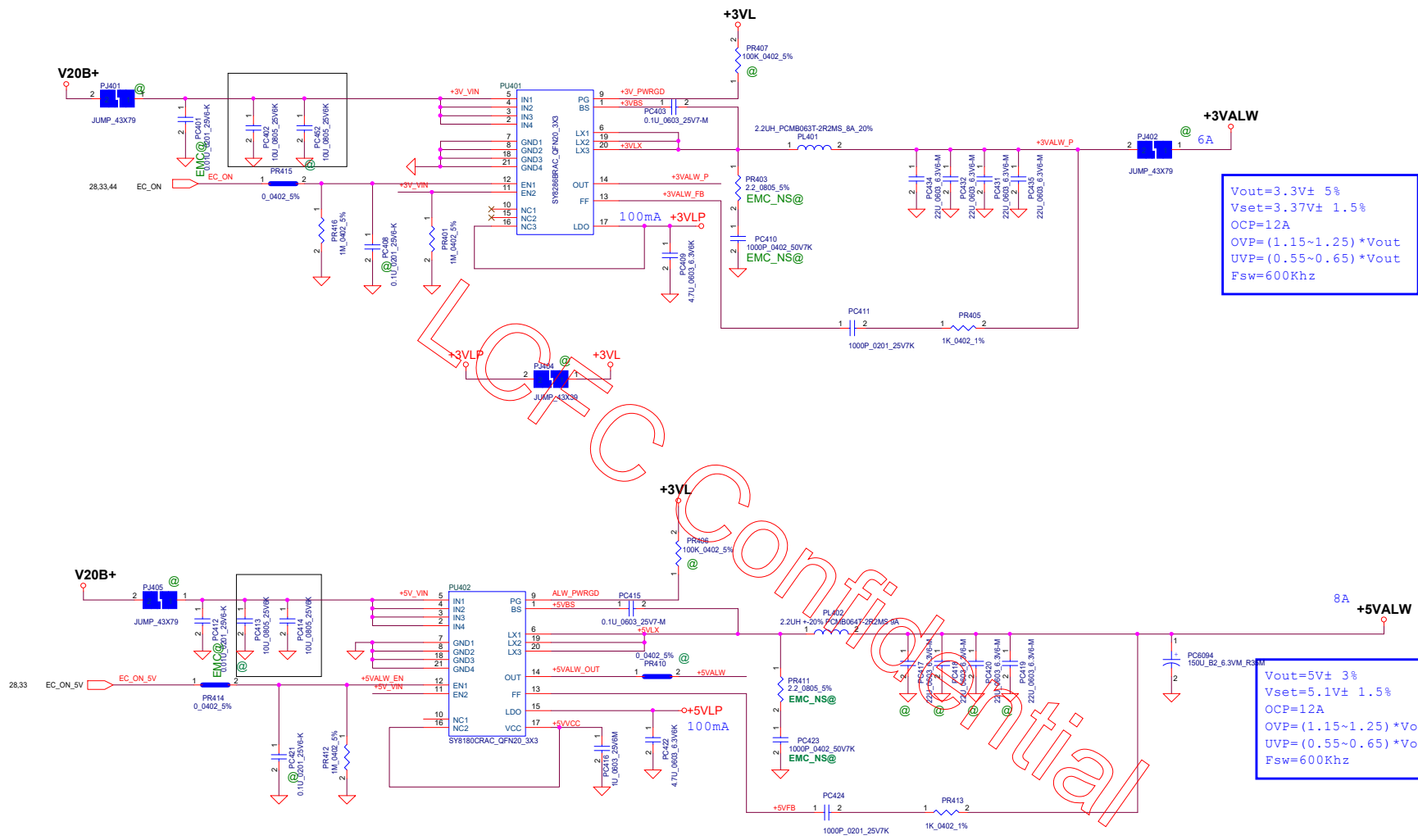




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Rev 1.0



$V_{out}=3.3V \pm 5\%$
 $V_{set}=3.37V \pm 1.5\%$
 $OC_P=12A$
 $OVP=(1.15 \sim 1.25) * V_{out}$
 $UVP=(0.55 \sim 0.65) * V_{out}$
 $F_{sw}=600Khz$

$V_{out}=5V \pm 3\%$
 $V_{set}=5.1V \pm 1.5\%$
 $OC_P=12A$
 $OVP=(1.15 \sim 1.25) * V_{out}$
 $UVP=(0.55 \sim 0.65) * V_{out}$
 $F_{sw}=600Khz$

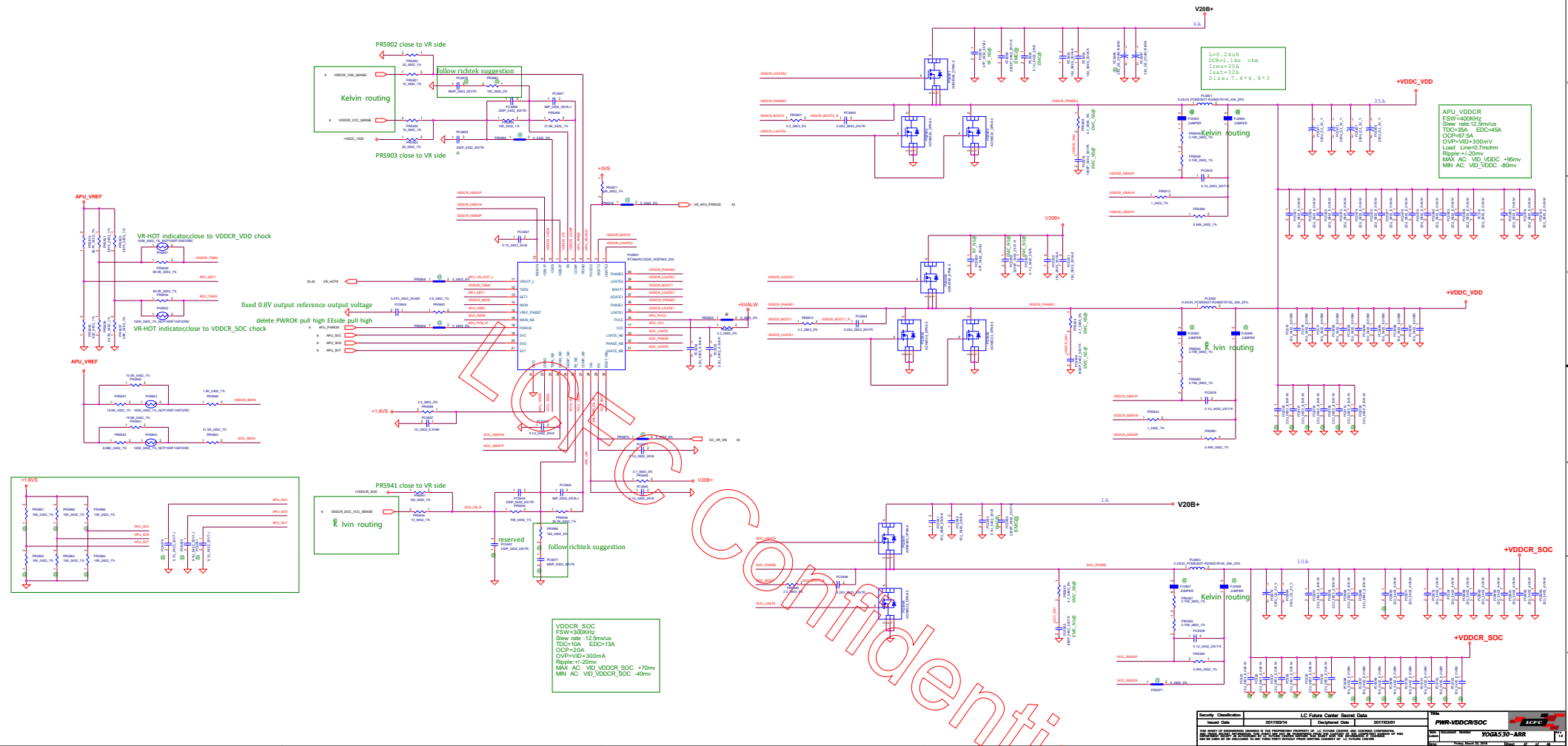
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